

## 100V N-Channel Enhancement Mode MOSFET

### Description

The APG40N10D uses advanced **APM-SGT11** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 40A$

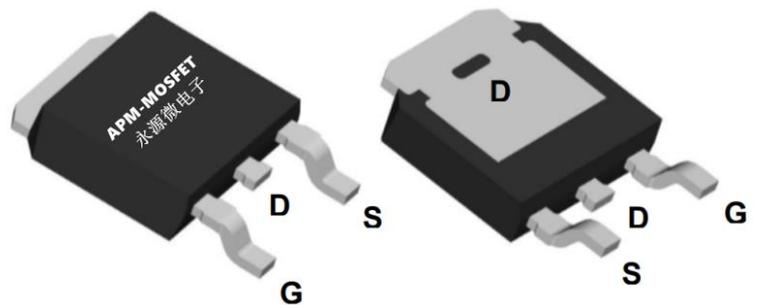
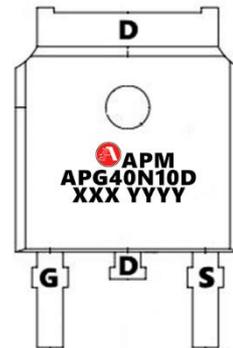
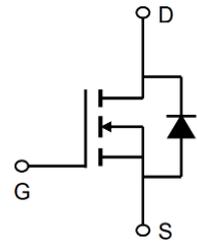
$R_{DS(ON)} < 17m\Omega$  @  $V_{GS}=10V$  (Type: **12.8mΩ**)

### Application

DC/DC Converter

LED Backlighting

Power Management Switches



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
APG40N10D	TO-252-3L	APG40N10D XXX YYYY	2500

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	40	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	28.5	A
IDM	Pulsed Drain Current	180	A
EAS	Single Pulse Avalanche Energy	180	mJ
IAS	Avalanche Current	12	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	67.5	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient	1.85	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case	62	$^\circ\text{C/W}$



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### Electrical Characteristics ( $T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BVDSS	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	108	-	V
IDSS	Drain-Source Leakage Current	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1	$\mu A$
IGSS	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.7	2.6	V
RDS(on)	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 15A$	-	12.8	17	m $\Omega$
		$V_{GS} = 4.5V, I_D = 10A$	-	15.5	20	m $\Omega$
$g_{fs}$	Forward Threshold Voltage	$V_{DS} = 10V, I_D = 20A$	-	54	-	S
$R_g$	Gate Resistance	$V_{DS} = V_{GS} = 0V, f = 1.0\text{MHz}$	-	1.75	-	$\Omega$
Ciss	Input Capacitance	$V_{DS} = 50V, V_{GS} = 0V, f = 1.0\text{MHz}$	-	1108	-	pF
Coss	Output Capacitance		-	154	-	pF
Crss	Reverse Transfer Capacitance		-	10.3	-	pF
$Q_g$	Total Gate Charge	$V_{DS} = 50V, I_D = 20A, V_{GS} = 10V$	-	22.5	-	nC
$Q_{gs}$	Gate-Source Charge		-	3	-	
$Q_{gd}$	Gate-Drain("Miller") Charge		-	5	-	
td(on)	Turn-On Delay Time	$V_{DS} = 50V, I_D = 20A, R_G = 3\Omega, V_{GS} = 10V$	-	8.6	-	ns
$t_r$	Turn-On Rise Time		-	3.6	-	
td(off)	Turn-Off Delay Time		-	23.6	-	
$t_f$	Turn-Off Fall Time		-	4.8	-	
$I_s$	Continuous Source Current		-	-	40	A
VSD	Diode Forward Voltage	$I_s = 20A, V_{GS} = 0V$	-	0.75	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 20A, dI_{SD}/dt = 100A/\mu s$	-	33	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	42	-	nC

#### Notes:

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、 The EAS data shows Max. rating . The test condition is  $V_{DD} = 50V, V_{GS} = 10V, L = 0.5\text{mH}, I_{AS} = 12A$
- 4、 The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5、 The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

Typical Characteristics

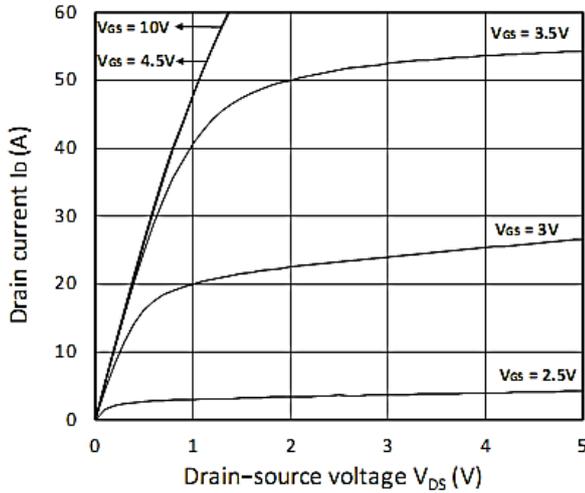


Figure 1. Output Characteristics

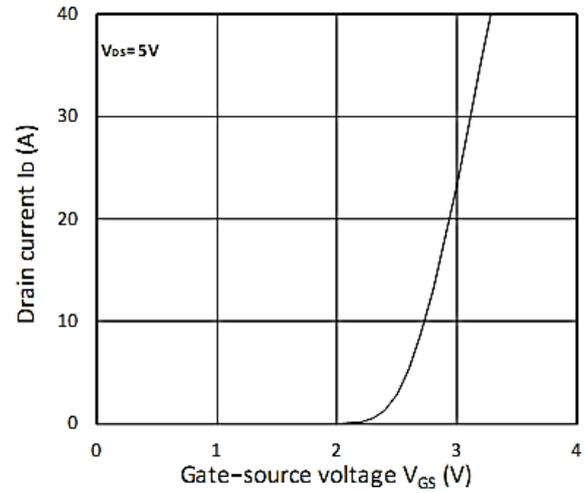


Figure 2. Transfer Characteristics

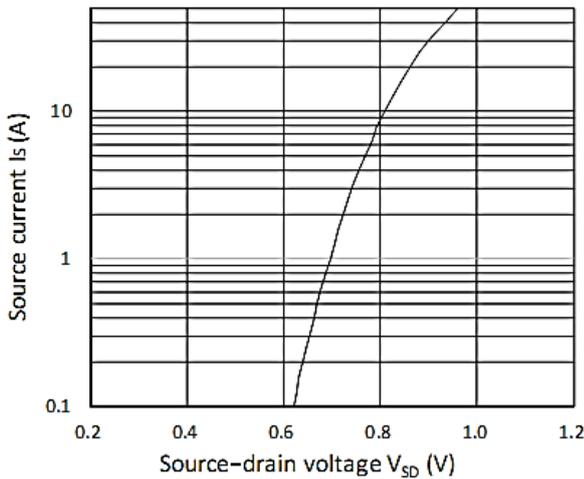


Figure 3. Forward Characteristics of Reverse

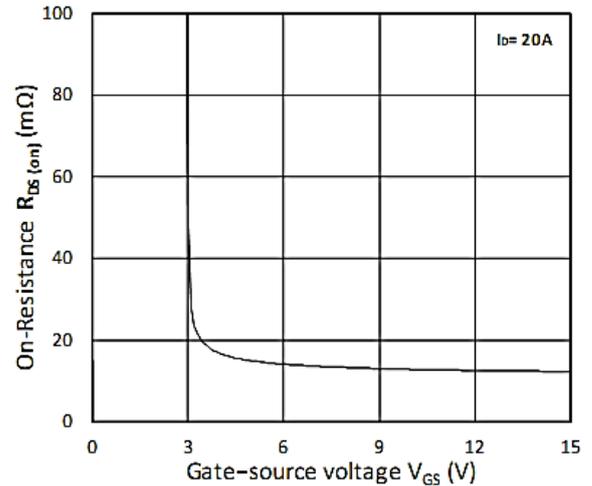


Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$

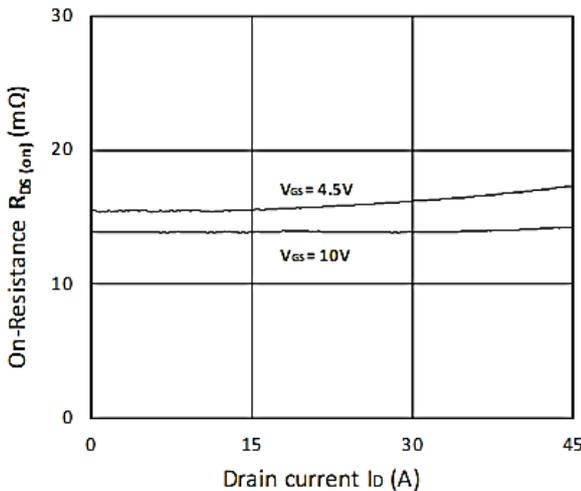


Figure 5.  $R_{DS(ON)}$  vs.  $I_D$

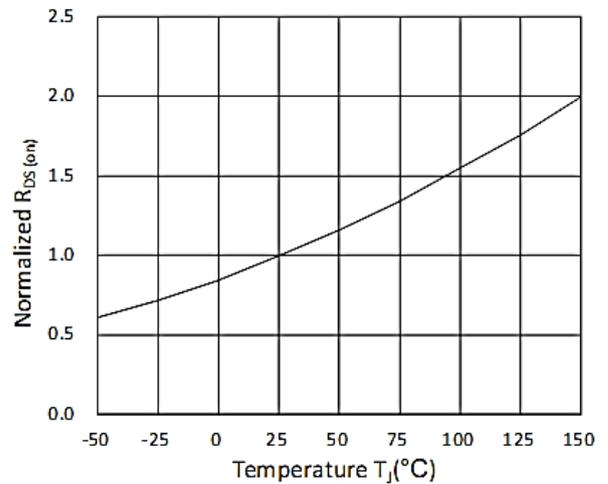


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature



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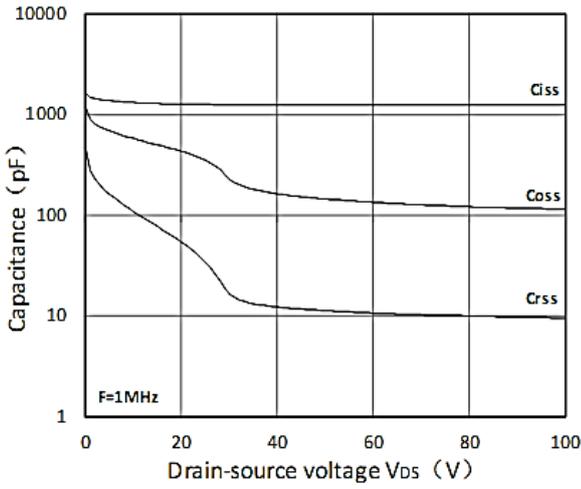


Figure 7. Capacitance Characteristics

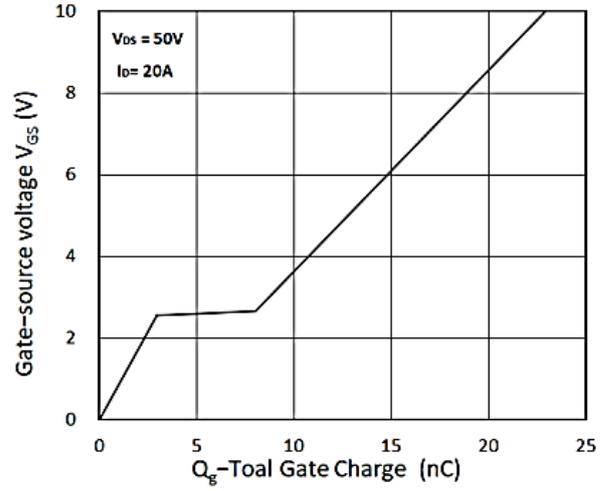


Figure 8. Gate Charge Characteristics

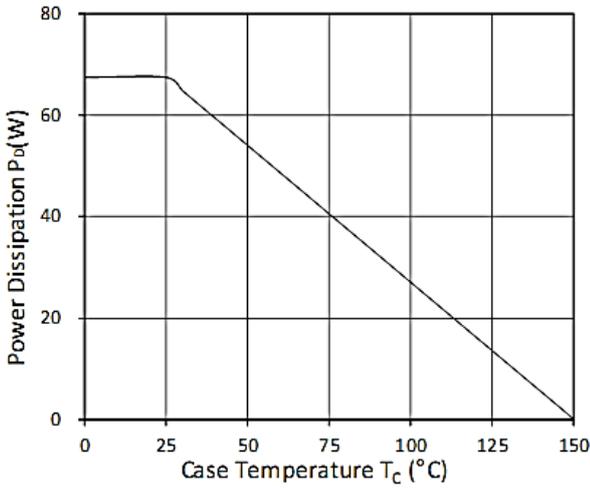


Figure 9. Power Dissipation

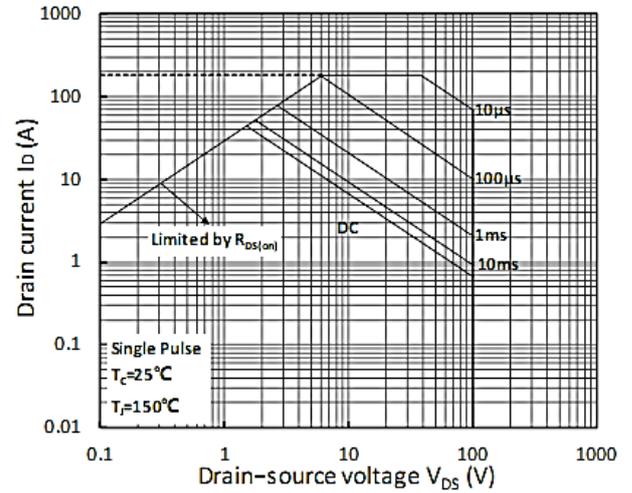


Figure 10. Safe Operating Area

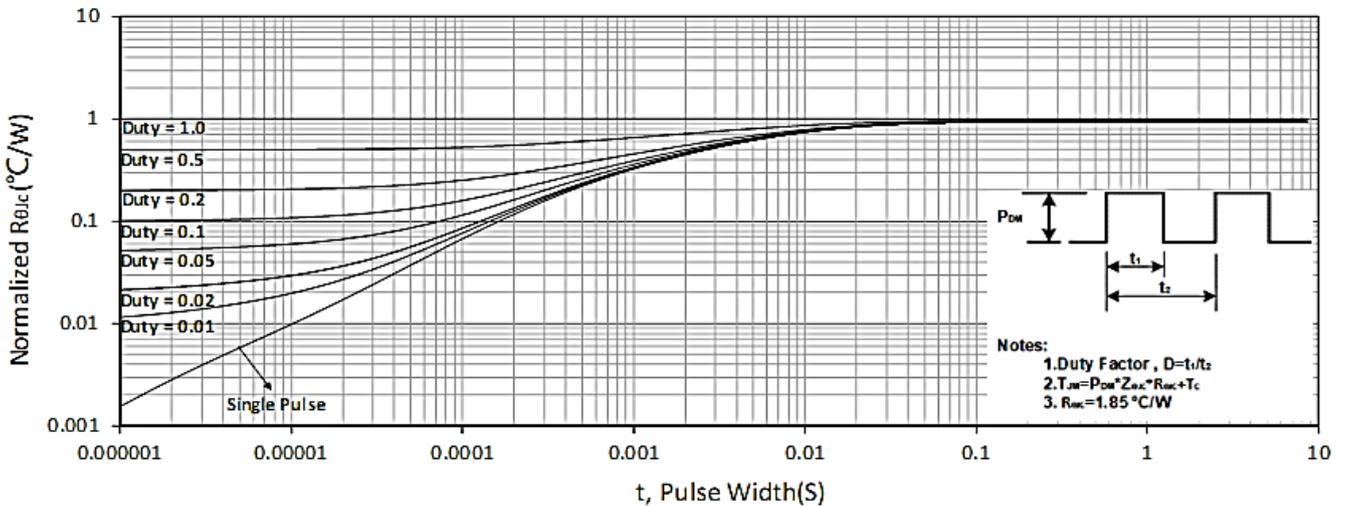
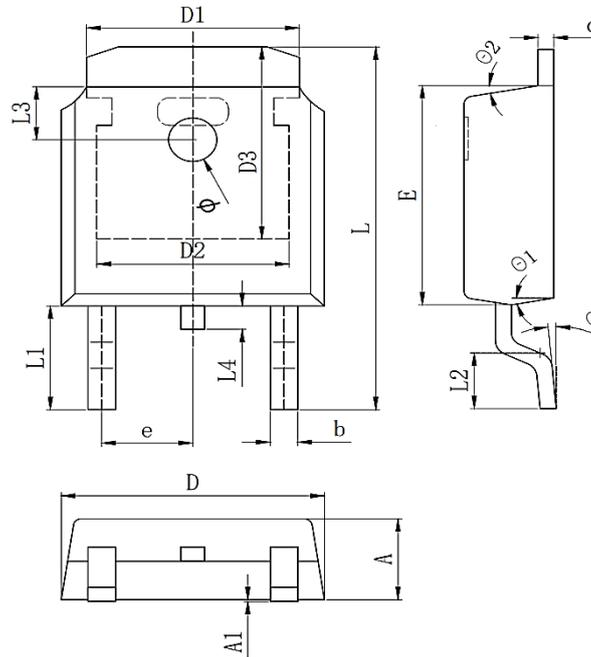


Figure 9 Normalized Maximum Transient Thermal Impedance

### Package Mechanical Data-TO-252-3L



Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
φ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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Edition	Date	Change
REV1.0	2018/11/10	Initial release
REV2.0	2020/4/25	Reduce RDS(on) and Ciss
REV2.1	2024/5/21	Reduce RDS(on)

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