

## 40V N+P-Channel Enhancement Mode MOSFET

### Description

The AP8G04S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 8.8A$

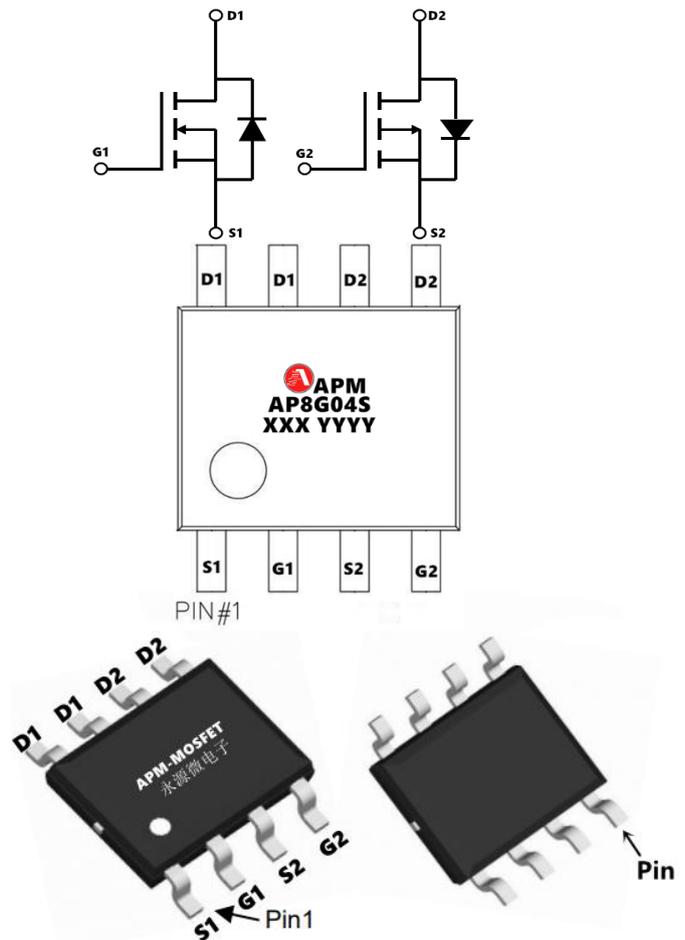
$R_{DS(ON)} < 28m\Omega$  @  $V_{GS}=10V$  (Type: 20m $\Omega$ )

$V_{DS} = -40V$   $I_D = -7.5A$

$R_{DS(ON)} < 42m\Omega$  @  $V_{GS}=-10V$  (Type: 35m $\Omega$ )

### Application

- Wireless charging
- Boost driver
- Brushless motor



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8G04S	SOP-8	AP8G04S XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
$V_{DS}$	Drain-Source Voltage	40	-40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.8	-7.5	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5.0	-4.2	A
IDM	Pulsed Drain Current <sup>2</sup>	20	-20	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	15	35	mJ
$P_D @ T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	1.67		W
TSTG	Storage Temperature Range	-55 to 150		$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	35		$^\circ C/W$

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### N-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$	-	-	1.0	$\mu A$
IGSS	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	$V_{GS}=10V, I_D=8A$	-	20	28	m $\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	25	35	m $\Omega$
Ciss	Input Capacitance	$V_{DS}=20V, V_{GS}=0V,$ $f=1.0MHz$	-	633	-	pF
Coss	Output Capacitance		-	67	-	pF
Crss	Reverse Transfer Capacitance		-	58	-	pF
Qg	Total Gate Charge	$V_{DS}=20V, I_D=8A,$ $V_{GS}=10V$	-	12	-	nC
Qgs	Gate-Source Charge		-	3.2	-	nC
Qgd	Gate-Drain("Miller") Charge		-	3.1	-	nC
td(on)	Turn-on Delay Time	$V_{DD}=20V, R_L=2.5\Omega$ $V_{GS}=10V, R_{REN}=3\Omega$	-	4	-	ns
tr	Turn-on Rise Time		-	3	-	ns
td(off)	Turn-off Delay Time		-	15	-	ns
tf	Turn-off Fall Time		-	2	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	8	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	32	A
VSD	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=8A$	-	-	1.2	V

#### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、 The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=8A$
- 4、 The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
- 5、 The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

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### P-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

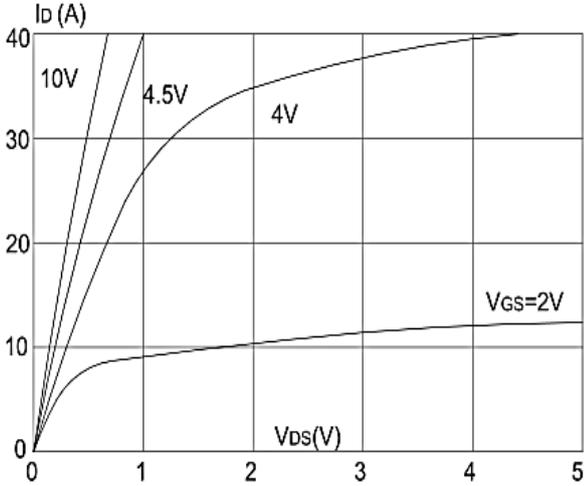
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	$\mu A$
IGSS	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
RDS(on)	Static Drain-Source on-Resistance	$V_{GS}=-10V, I_D=-8A$	-	35	42	m $\Omega$
		$V_{GS}=-4.5V, I_D=-5A$	-	46	62	
Ciss	Input Capacitance	$V_{DS}=-20V, V_{GS}=0V, f=1.0\text{MHz}$	-	1034	-	pF
Coss	Output Capacitance		-	107	-	pF
Crss	Reverse Transfer Capacitance		-	79.5	-	pF
Qg	Total Gate Charge	$V_{DS}=-20V, I_D=-5A, V_{GS}=-10V$	-	20	-	nC
Qgs	Gate-Source Charge		-	3.5	-	nC
Qgd	Gate-Drain("Miller") Charge		-	4.2	-	nC
td(on)	Turn-on Delay Time	$V_{DD}=-20V, I_D=-5A, V_{GS}=-10V, R_{GEN}=2.5\Omega$	-	8	-	ns
tr	Turn-on Rise Time		-	15	-	ns
td(off)	Turn-off Delay Time		-	23	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	9	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-10	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-40	A
VSD	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=-10A$	-	-	-1.2	V
trr	Reverse Recovery Time	$T_J=25^\circ\text{C}, I_F=10A, dI/dt=100A/\mu s$	-	29	-	ns
Qrr	Reverse Recovery Charge		-	20	-	nC

**Note :**

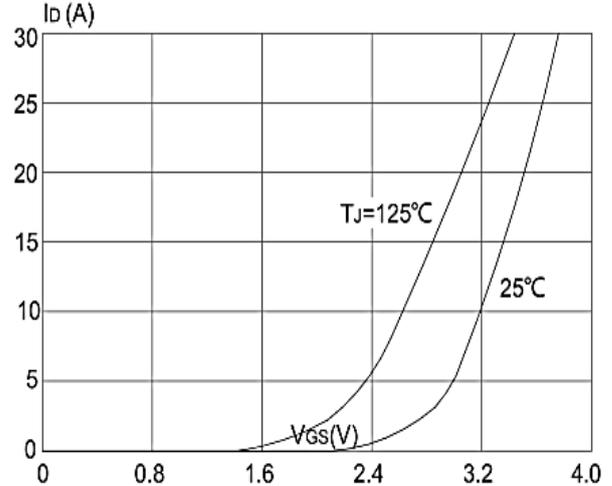
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- 3、The EAS data shows Max. rating. The test condition is  $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-8A$
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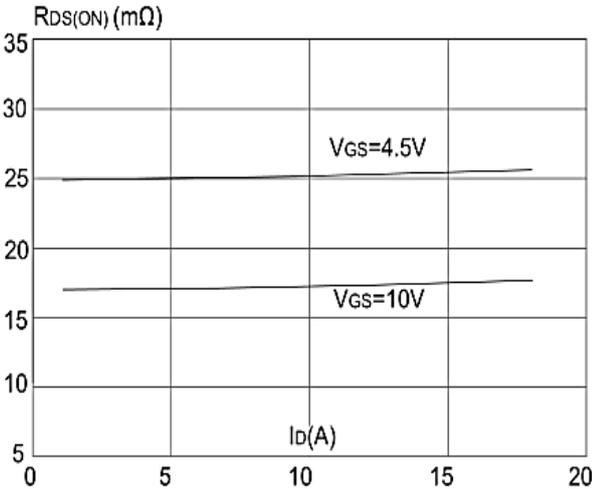
**N-Typical Characteristics**



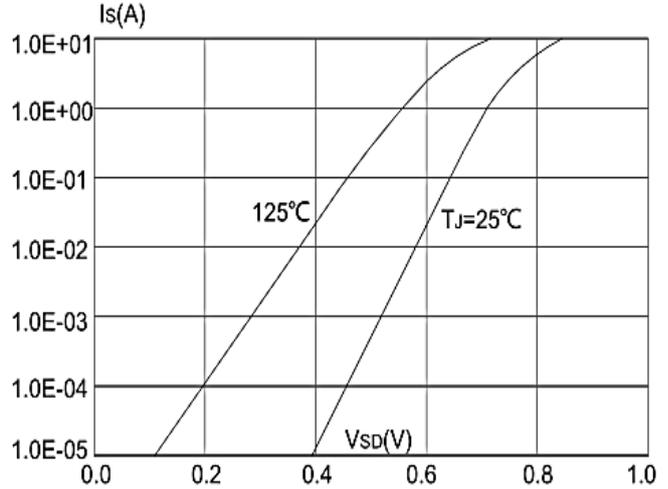
**Figure 1: Output Characteristics**



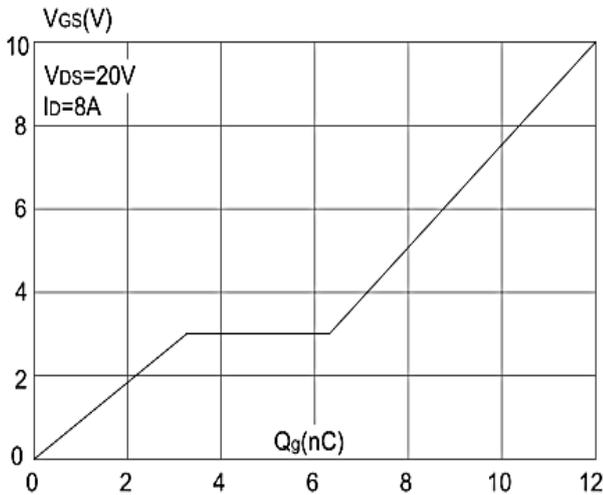
**Figure 2: Typical Transfer Characteristics**



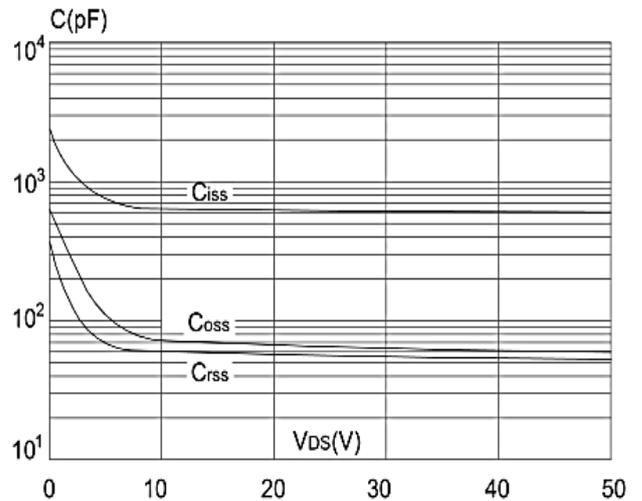
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**



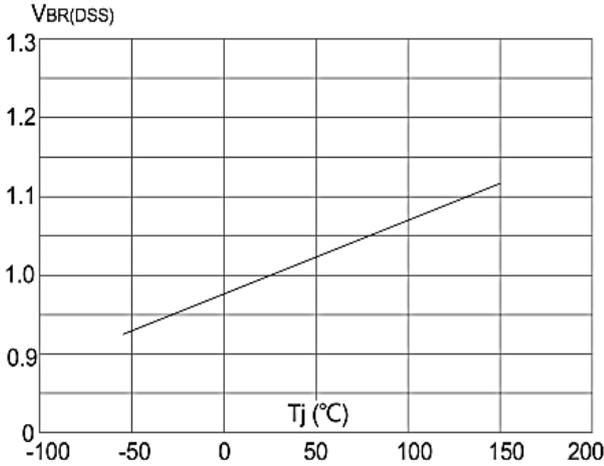
**Figure 5: Gate Charge Characteristics**



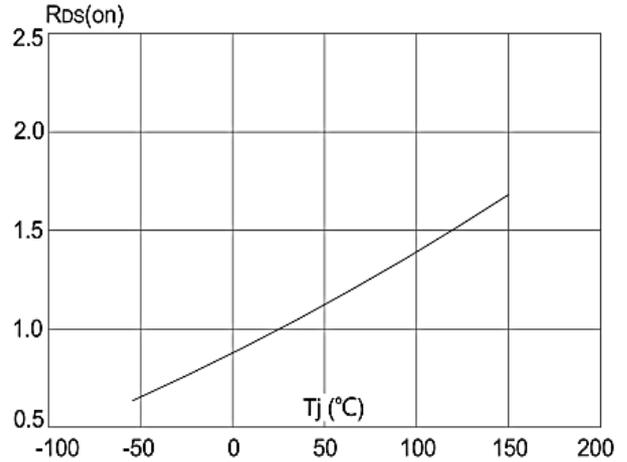
**Figure 6: Capacitance Characteristics**



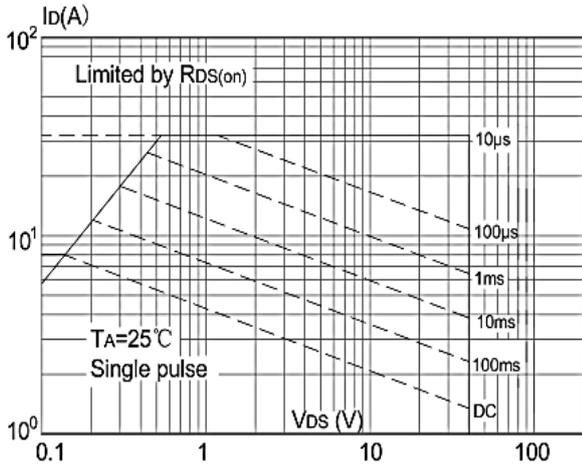
**40V N+P-Channel Enhancement Mode MOSFET**



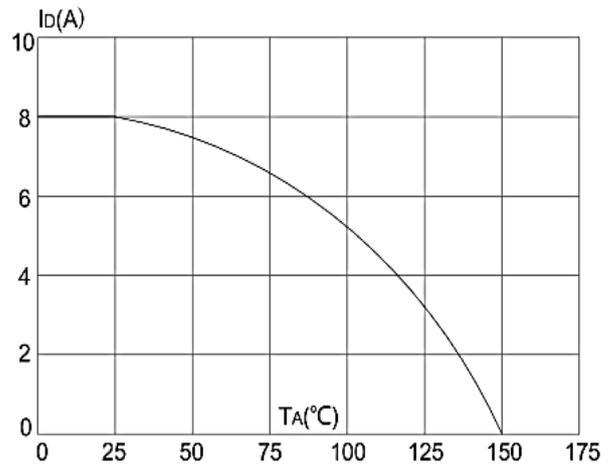
**Figure 7: Normalized Breakdown Voltage vs Junction Temperature**



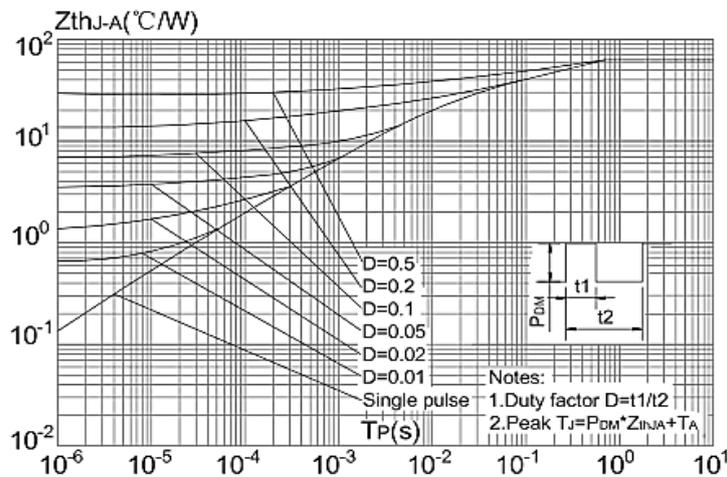
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area**



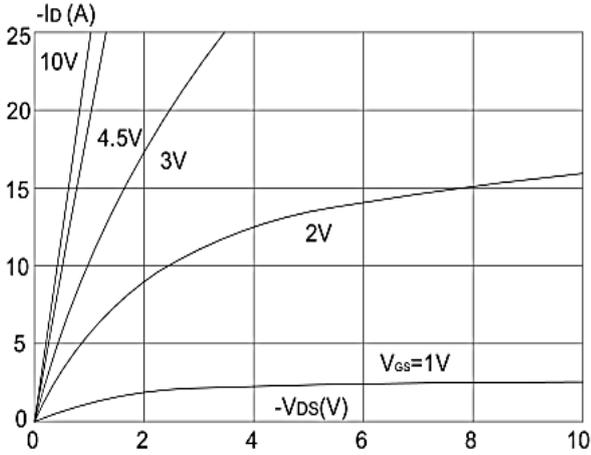
**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



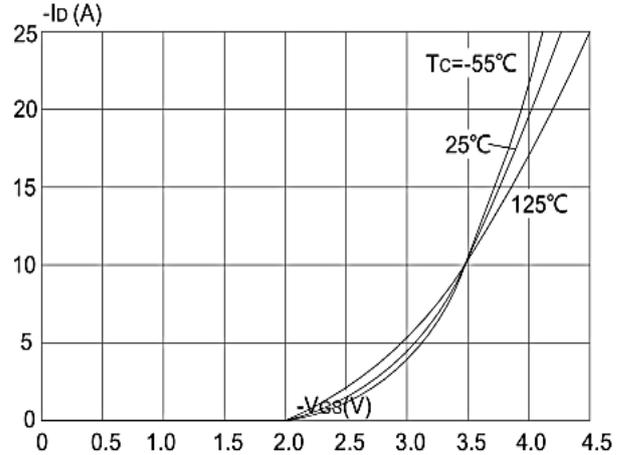
**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien**

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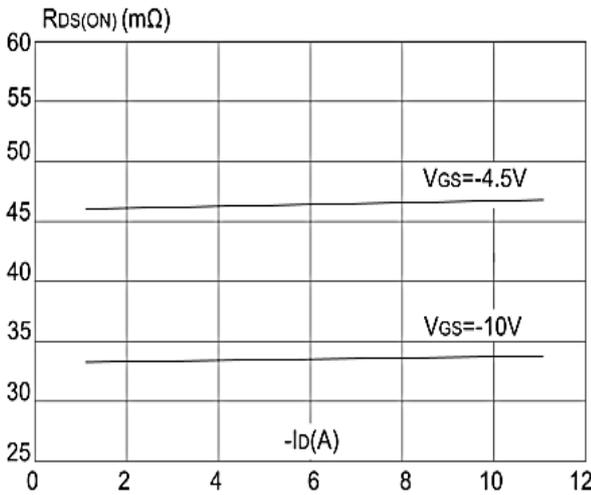
**P-Typical Characteristics**



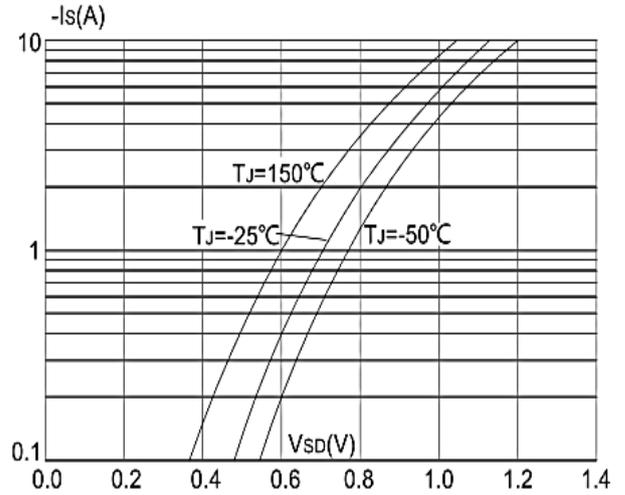
**Figure 1: Output Characteristics**



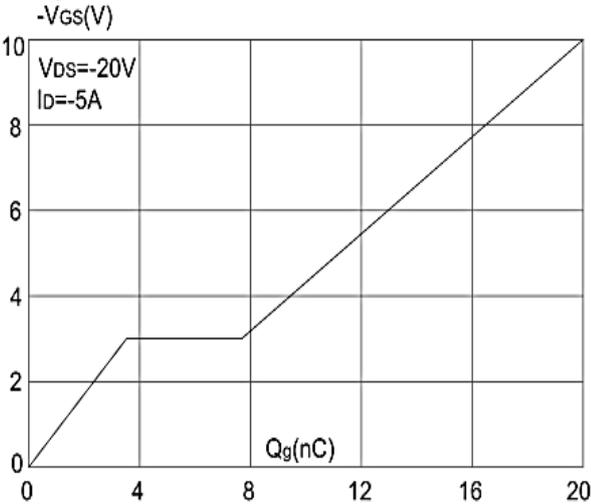
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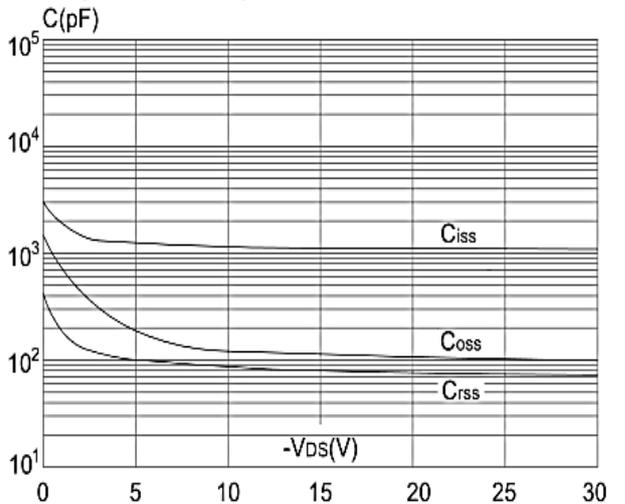
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**



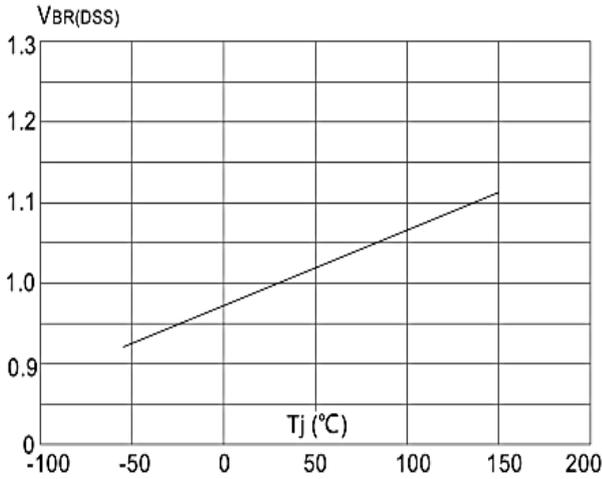
**Figure 5: Gate Charge Characteristics**



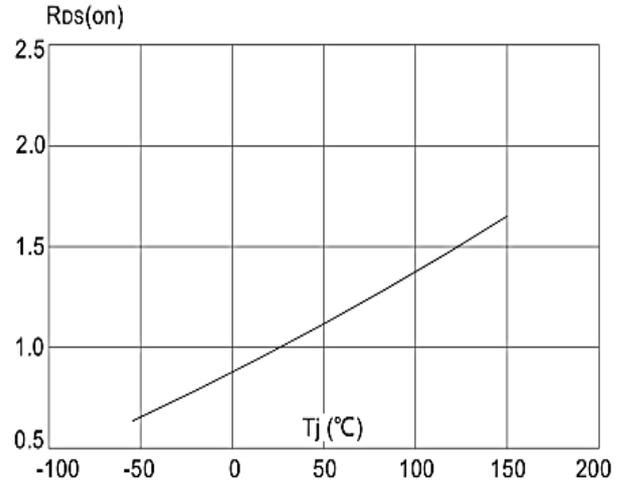
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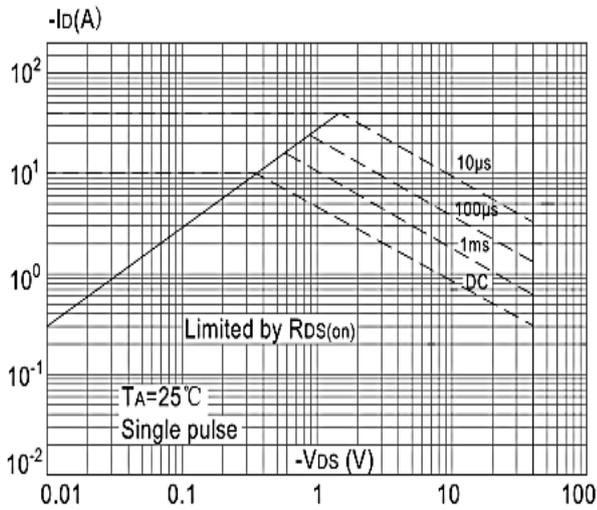
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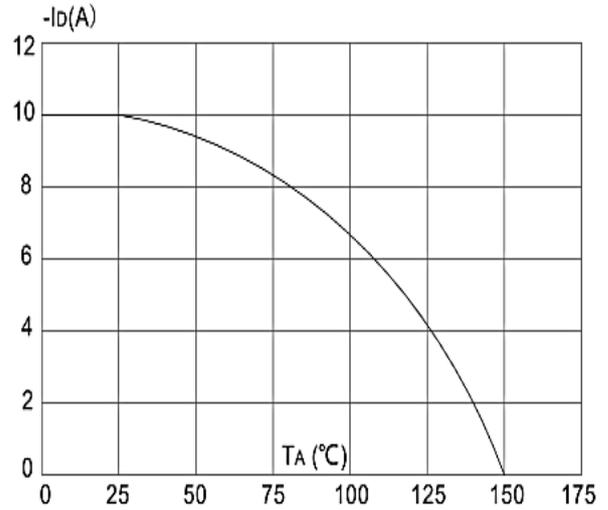
**Figure 7: Normalized Breakdown Voltage vs Junction Temperature**



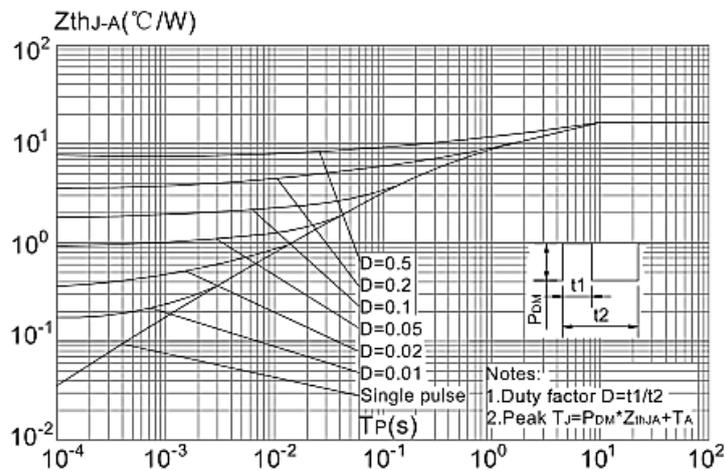
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area**



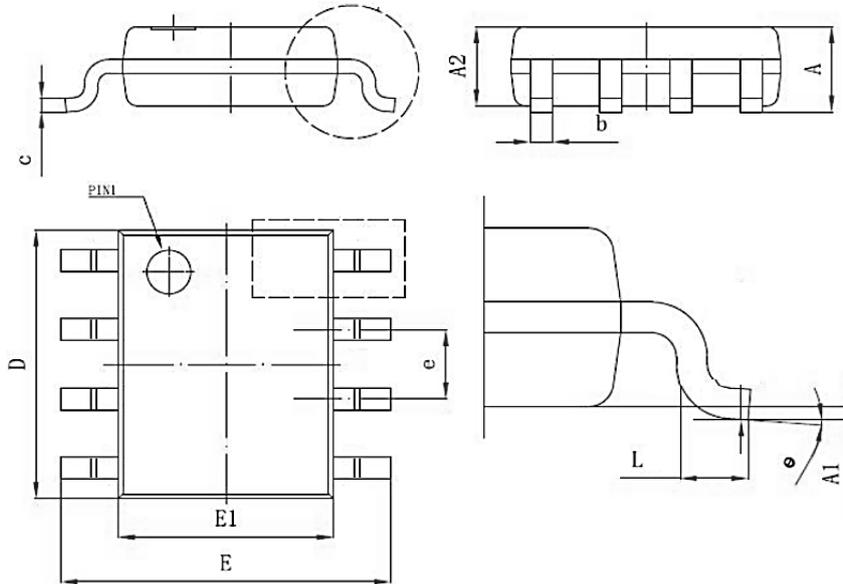
**Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien**



Package Mechanical Data-SOP-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	1.35	1.55	1.75
A1	0.02	0.15	0.25
A2	1.425	1.45	1.475
b	0.3	0.4	0.5
c	0.15	0.2	0.25
D	4.8	5	5.2
E	5.8	6	6.2
E1	3.8	4	4.2
e	1.27BSC		
L	0.4		1.27
θ	0°		8°

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Edition	Date	Change
REV1.0	2019/5/31	Initial release
REV1.1	2024/5/12	Change logo and Reduce Rds

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