

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP8G02S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 8.5A$

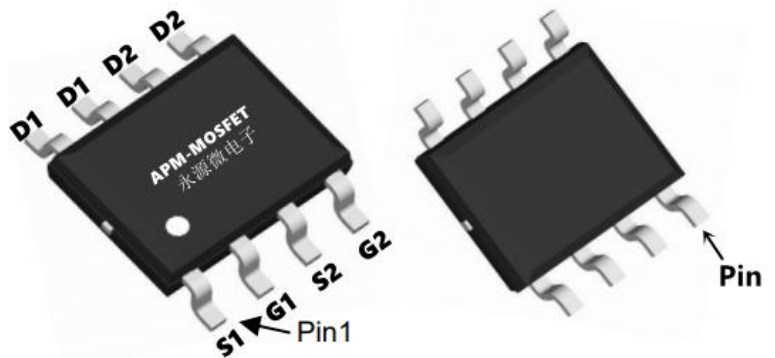
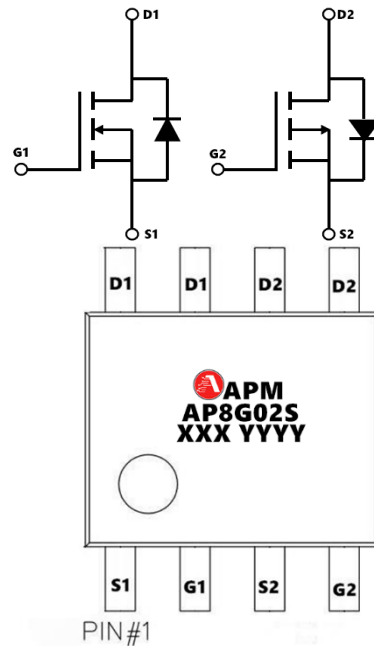
$R_{DS(ON)} < 35m\Omega$ @ $V_{GS}=10V$ (Type: 28m Ω)

$V_{DS} = -20V$ $I_D = -7.8A$

$R_{DS(ON)} < 38m\Omega$ @ $V_{GS}=-10V$ (Type: 28m Ω)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8G02S	SOP-8L	AP8G02S XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A = 25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.5	-7.8	A
$I_D @ T_A = 70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.2	-5.5	A
I_{DM}	Pulsed Drain Current ²	28	-32	A
E_{AS}	Single Pulse Avalanche Energy ³	24	78	mJ
$P_D @ T_A = 25^{\circ}C$	Total Power Dissipation ⁴	1.5	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150		$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150		$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85		$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	50		$^{\circ}C/W$

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P-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	22	---	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =3A	---	28	35	mΩ
		V _{GS} =2.5V, I _D =2A	---	32	40	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	0.5	0.75	1.2	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =16V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =16V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =3A	---	10.5	---	S
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =3A	---	4.6	---	nC
Q _{gs}	Gate-Source Charge		---	0.7	---	
Q _{gd}	Gate-Drain Charge		---	1.5	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =10V, V _{GS} =4.5V, R _G =3.3Ω, I _D =3A	---	1.6	---	ns
T _r	Rise Time		---	42	---	
T _{d(off)}	Turn-Off Delay Time		---	14	---	
T _f	Fall Time		---	7	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	310	---	pF
C _{oss}	Output Capacitance		---	49	---	
C _{rss}	Reverse Transfer Capacitance		---	35	---	
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	3.6	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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P-Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	-24	-	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$	-	-	-1	μA
IGSS	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 12V$	-	-	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.7	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	$V_{GS}=-4.5V, I_D=-4.1A$	-	28	35	m Ω
RDS(on)	Static Drain-Source on-Resistance note2	$V_{GS}=-2.5V, I_D=-3A$	-	35	42	m Ω
Ciss	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V, f=1.0MHz$	-	830	-	pF
Coss	Output Capacitance		-	132	-	pF
Crss	Reverse Transfer Capacitance		-	85	-	pF
Qg	Total Gate Charge	$V_{DS}=-10V, I_D=-2A, V_{GS}=-4.5V$	-	8.8	-	nC
Qgs	Gate-Source Charge		-	1.4	-	nC
Qgd	Gate-Drain("Miller") Charge		-	1.9	-	nC
td(on)	Turn-on Delay Time	$V_{DD}=-10V, I_D=-3.3A, R_G=1\Omega, V_{GEN}=-4.5V$	-	10	-	ns
tr	Turn-on Rise Time		-	32	-	ns
td(off)	Turn-off Delay Time		-	50	-	ns
t _f	Turn-off Fall Time		-	51	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.1	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
VSD	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=-4.1A$	-	-	-1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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N-Channel Typical Characteristics

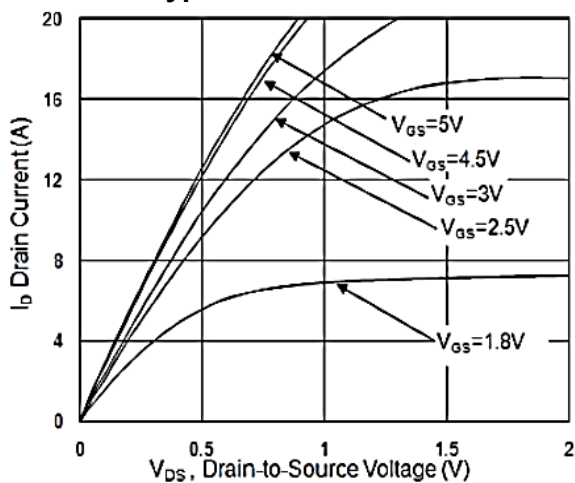


Fig.1 Typical Output Characteristics

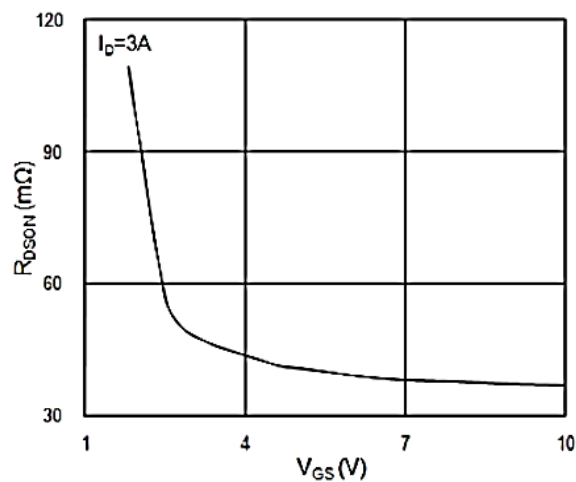


Fig.2 On-Resistance vs. G-S Voltage

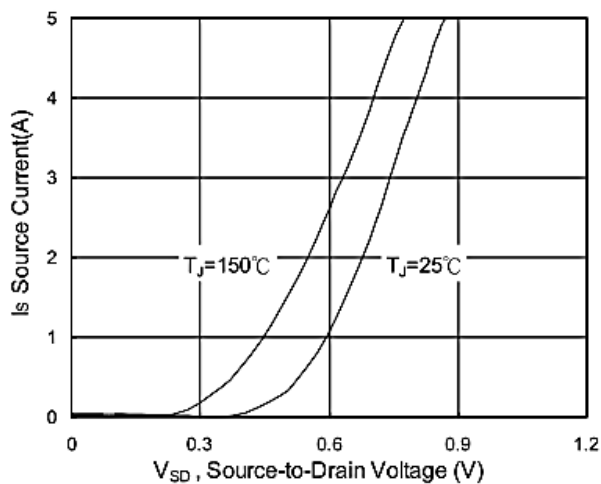


Fig.3 Source Drain Forward Characteristics

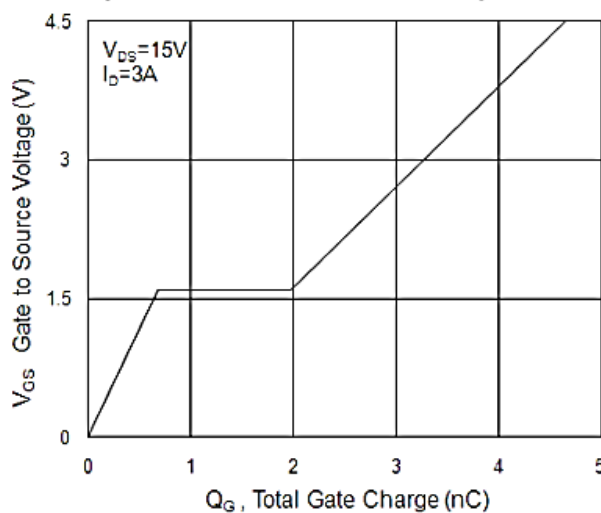


Fig.4 Gate-Charge Characteristics

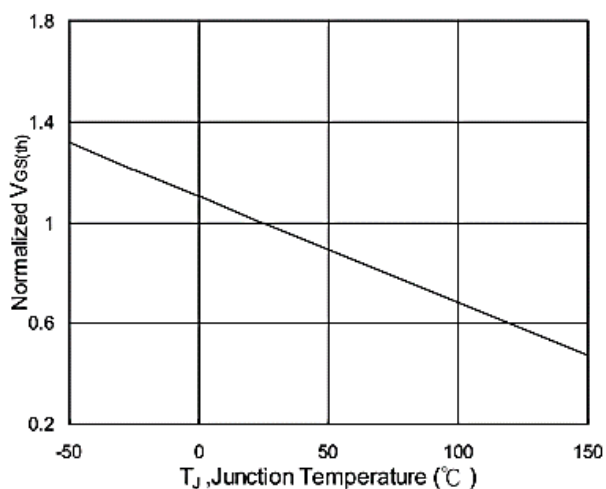


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

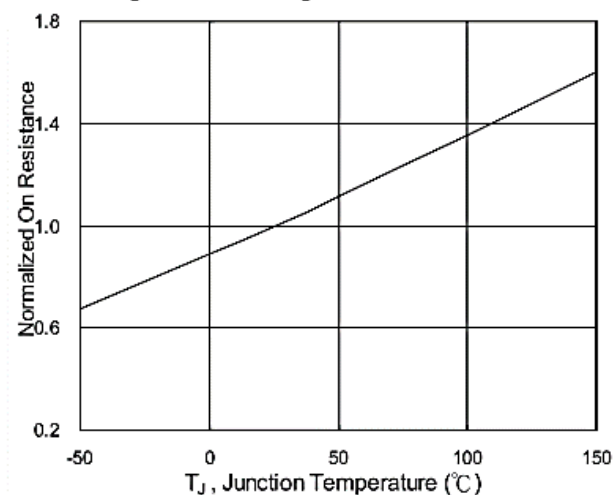


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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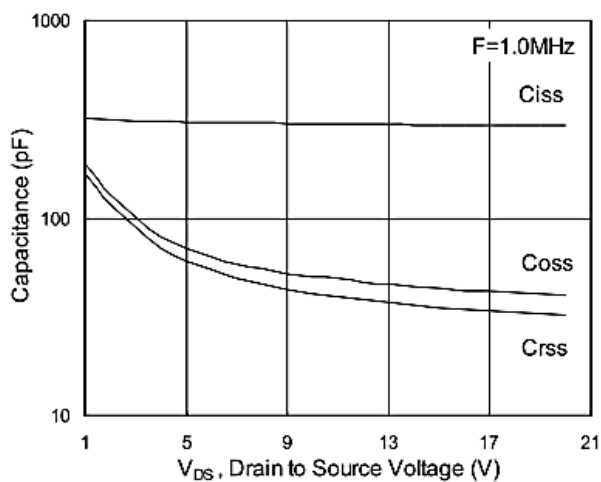


Fig.7 Capacitance

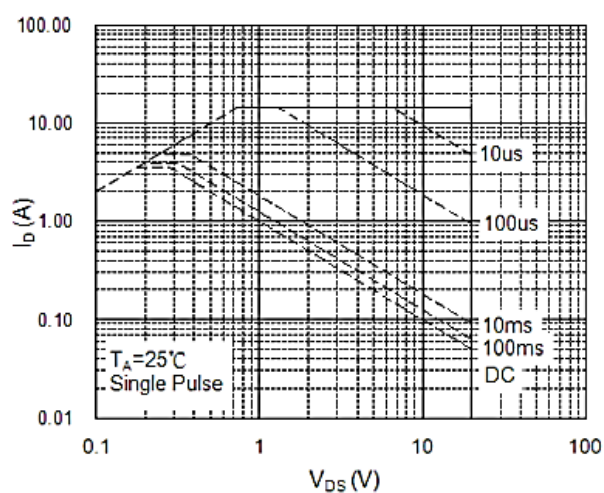


Fig.8 Safe Operating Area

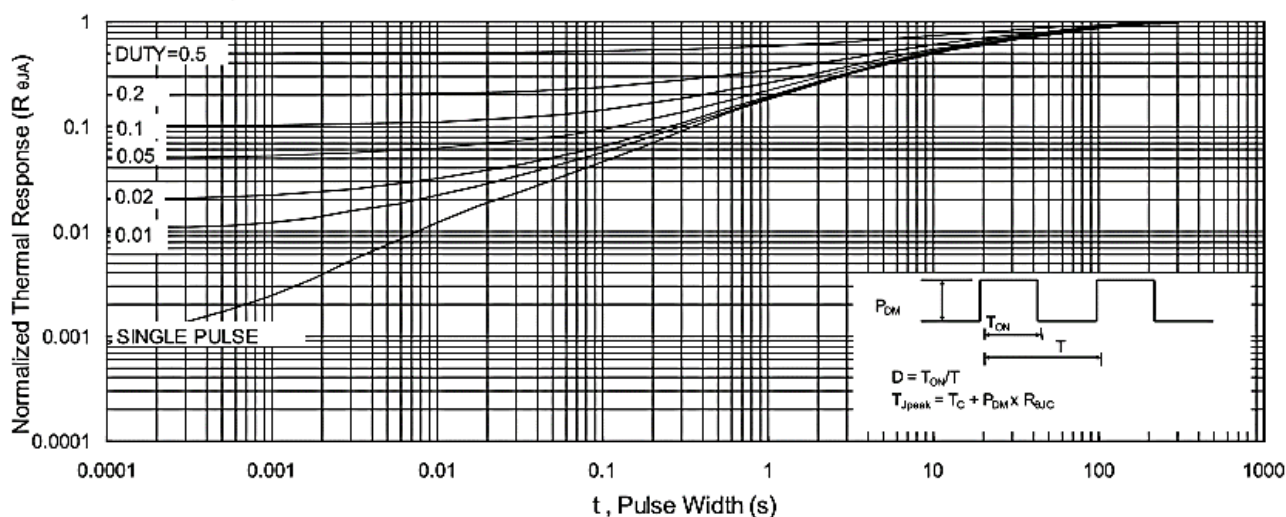


Fig.9 Normalized Maximum Transient Thermal Impedance

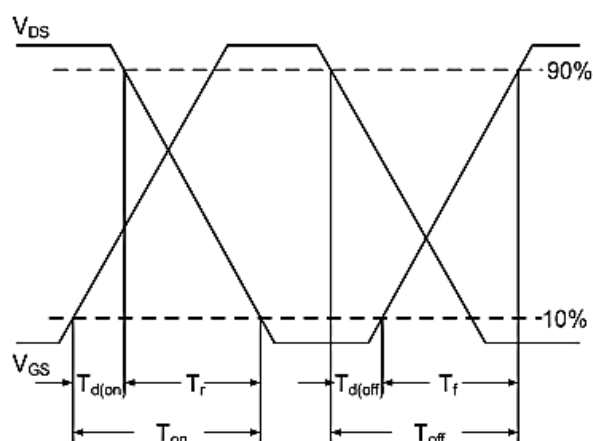


Fig.10 Switching Time Waveform

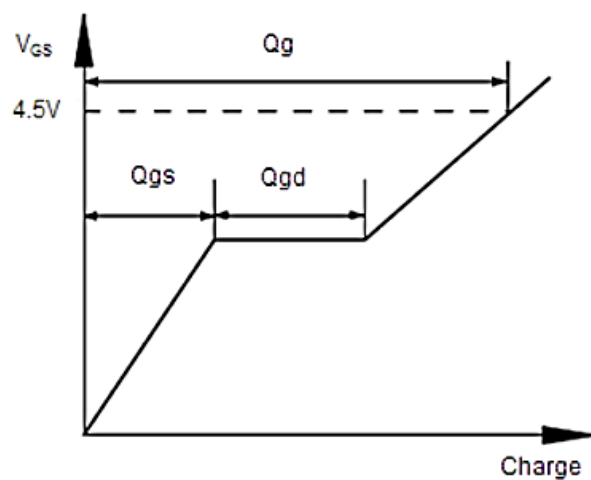


Fig.11 Gate Charge Waveform

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P-Channel Typical Characteristics

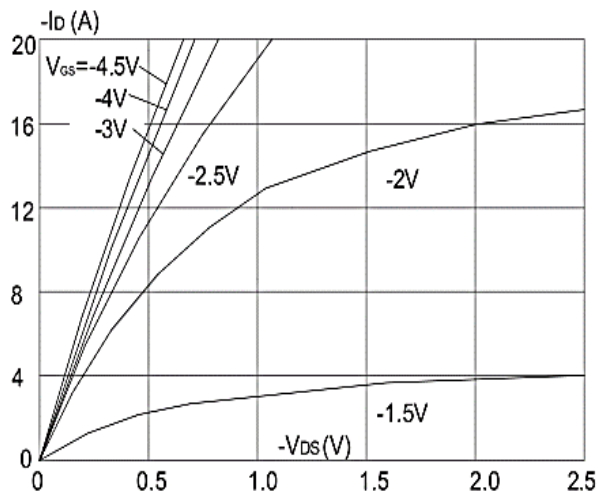


Figure1: Output Characteristics

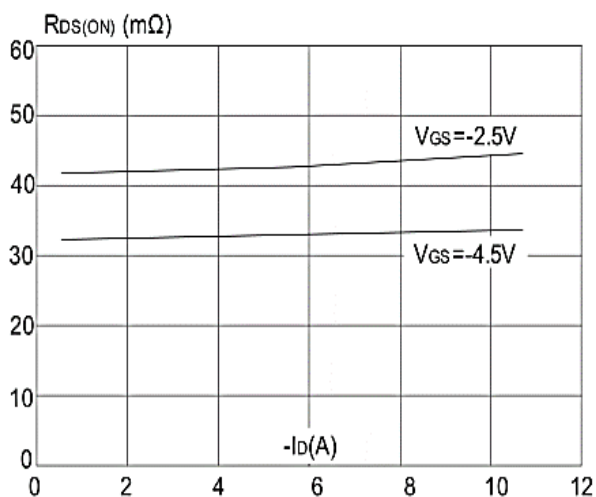


Figure 3:On-resistance vs. Drain Current

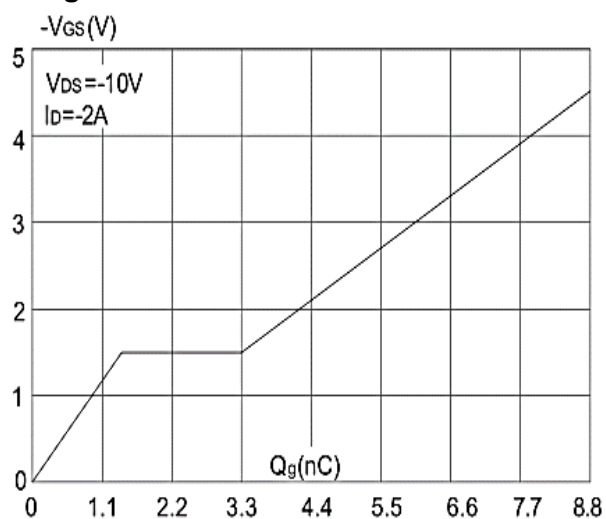


Figure 5: Gate Charge Characteristics

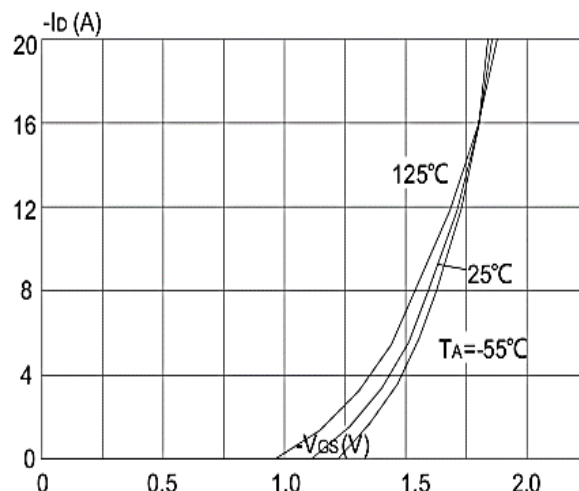


Figure 2: Typical Transfer Characteristics

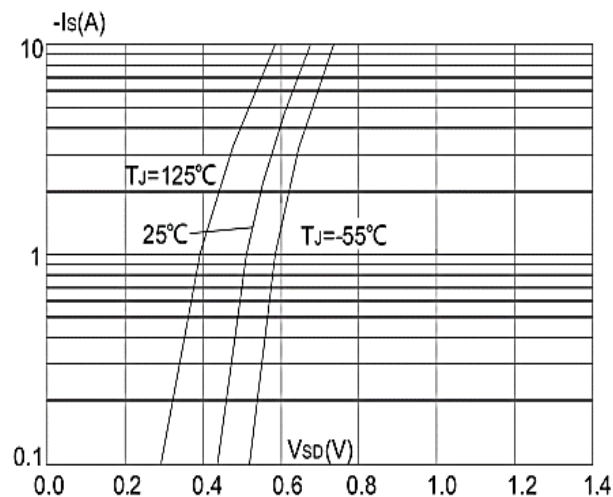


Figure 4: Body Diode Characteristics

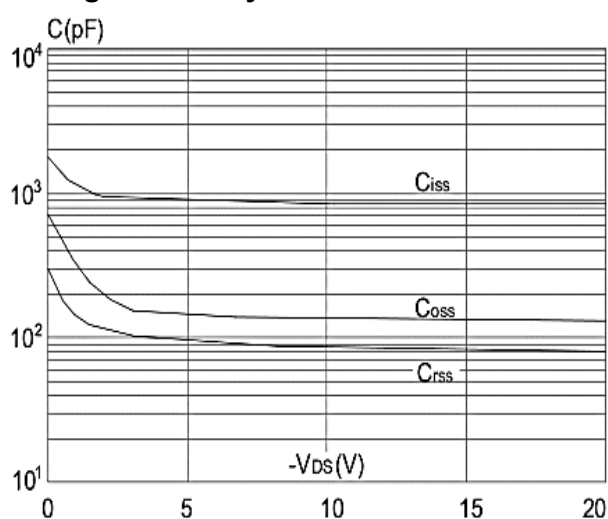


Figure 6: Capacitance Characteristics

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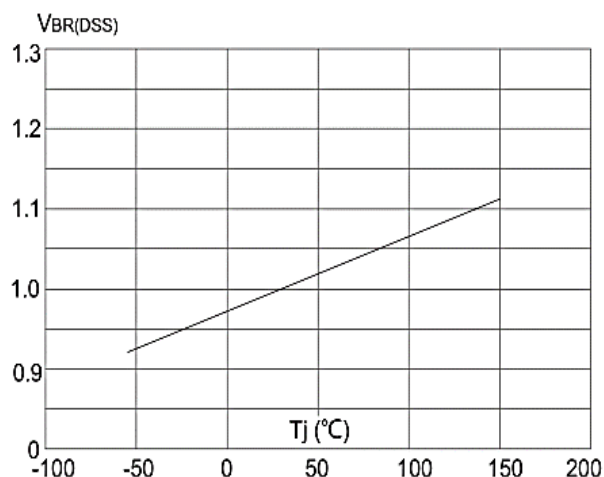


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

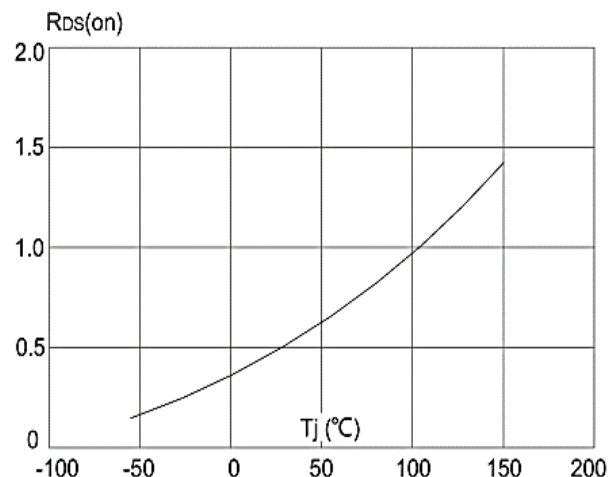


Figure 8: Normalized on Resistance vs. Junction Temperature

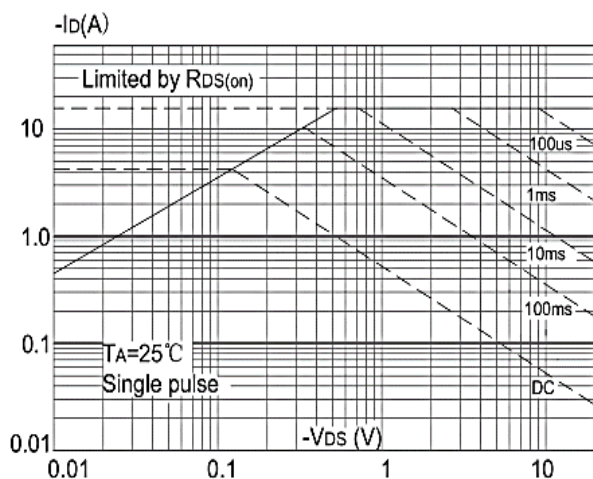


Figure 9: Maximum Safe Operating Area

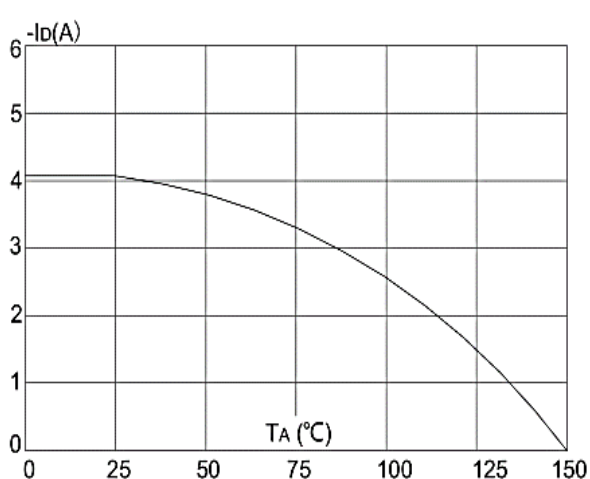


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

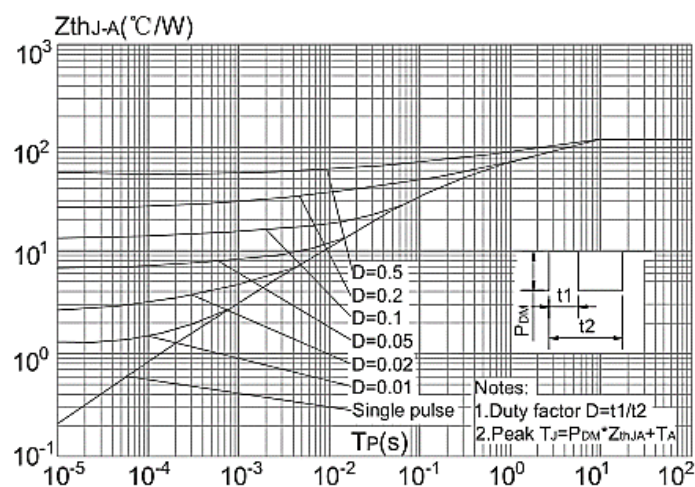
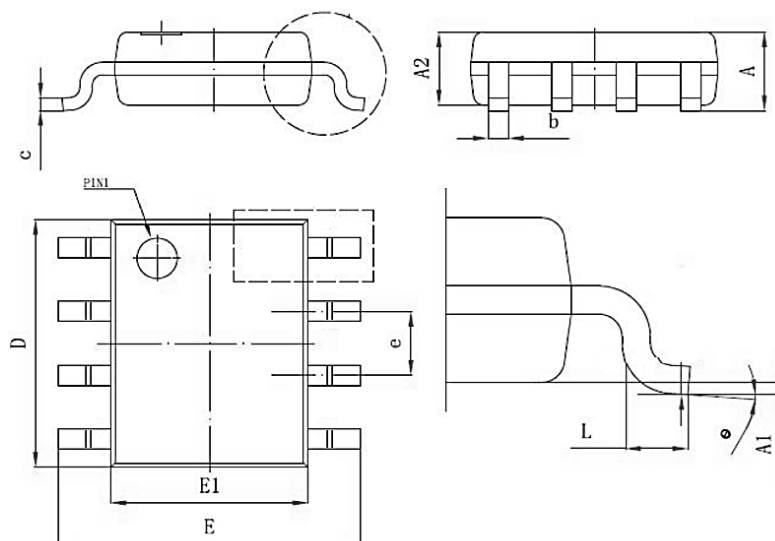


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Package Mechanical Data-SOP-8L-Double



Symbol	Dim in mm		
	Min	Typ	Max
A	1.35	1.55	1.75
A1	0.02	0.15	0.25
A2	1.425	1.45	1.475
b	0.3	0.4	0.5
c	0.15	0.2	0.25
D	4.8	5	5.2
E	5.8	6	6.2
E1	3.8	4	4.2
e	1.27BSC		
L	0.4		1.27
θ	0°		8°

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2022/9/21	Initial release

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