



永源微电子科技有限公司

AP8G02BLI

8A 20V N+P 高频无线充场效应管晶体管

简介:

AP8G02BLI 是一颗针对无线充 N+P 全桥高频电路高性价比产品，使用的是第三代沟槽技术，优化 N&P Ciss 电容数据和 RDS，具备超高的性价比。

适配主控型号:

国内所有市场主流 MCU 无线充方案系列。

市场应用:

磁吸无线充，移动电源 15W 无线充

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP8G02BLI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 8.5A$

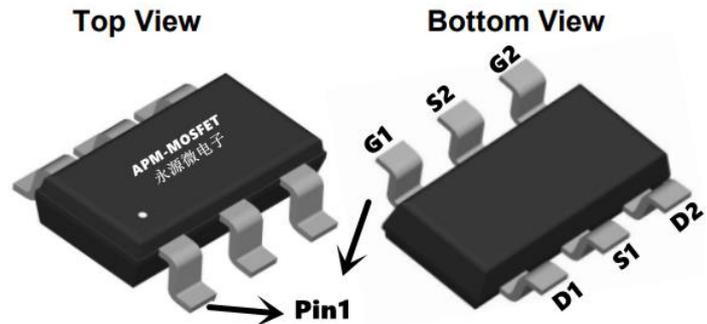
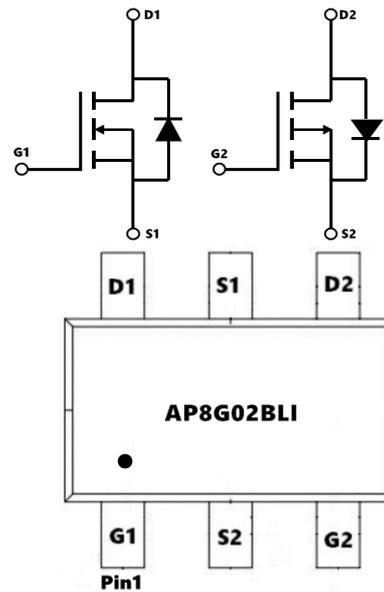
$R_{DS(ON)} < 28m\Omega$ @ $V_{GS}=4.5V$ (Type: 24m Ω)

$V_{DS} = -20V$ $I_D = -7.6A$

$R_{DS(ON)} < 35m\Omega$ @ $V_{GS}=-4.5V$ (Type: 29m Ω)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8G02BLI	SOT23-6L	AP8G02BLI	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.5	-7.6	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.2	-5.3	A
IDM	Pulsed Drain Current ²	28	-30	A
EAS	Single Pulse Avalanche Energy ³	24	76	mJ
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	1.5		W
TSTG	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	125		$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	52		$^\circ\text{C}/\text{W}$

20V N+P-Channel Enhancement Mode MOSFET

N-Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	22	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=3A$	---	24	28	m Ω
		$V_{GS}=2.5V, I_D=2A$	---	28	40	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.5	0.65	1.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=20V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=20V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=3A$	---	10.5	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=3A$	---	4.6	---	nC
Q_{gs}	Gate-Source Charge		---	0.7	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega, I_D=3A$	---	1.6	---	ns
T_r	Rise Time		---	42	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	7	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	310	---	pF
C_{oss}	Output Capacitance		---	49	---	
C_{riss}	Reverse Transfer Capacitance		---	35	---	
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V, \text{Force Current}$	---	---	3.6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、 The power dissipation is limited by 150 $^{\circ}\text{C}$ junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

20V N+P-Channel Enhancement Mode MOSFET
P-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDSS	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} = 0V	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	-	-	1.0	μA
IGSS	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.5	-0.6	-1.0	V
RDS(ON)	Static Drain-Source ON-Resistance ⁽³⁾	V _{GS} = -4.5V, I _D = -4A	-	29	35	mΩ
		V _{GS} = -2.5V, I _D = -3A	-	36	42	mΩ
Ciss	Input Capacitance	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz	-	534	-	pF
Coss	Output Capacitance		-	62	-	pF
Crss	Reverse Transfer Capacitance		-	50	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to -4.5V V _{DS} = -10V, I _D = -2A	-	5.6	-	nC
Q _{gs}	Gate Source Charge		-	1	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	1	-	nC
td(on)	Turn-On DelayTime	V _{GS} = -4.5V, V _{DD} = -10V I _D = -2A, R _{GEN} = 3Ω	-	5	-	ns
t _r	Turn-On Rise Time		-	21	-	ns
td(off)	Turn-Off DelayTime		-	110	-	ns
t _f	Turn-Off Fall Time		-	239	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-3	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-12	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = -4.2A	-	-	-1.2	V
trr	Body Diode Reverse Recovery Time	I _F = -2A, di/dt = 100A/us	-	64	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	10	-	nC

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

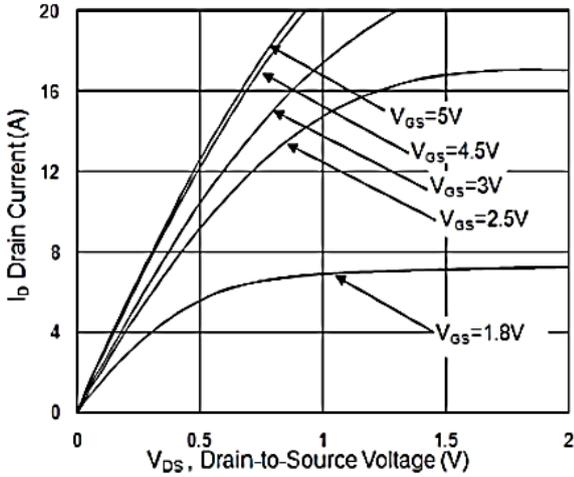


Fig.1 Typical Output Characteristics

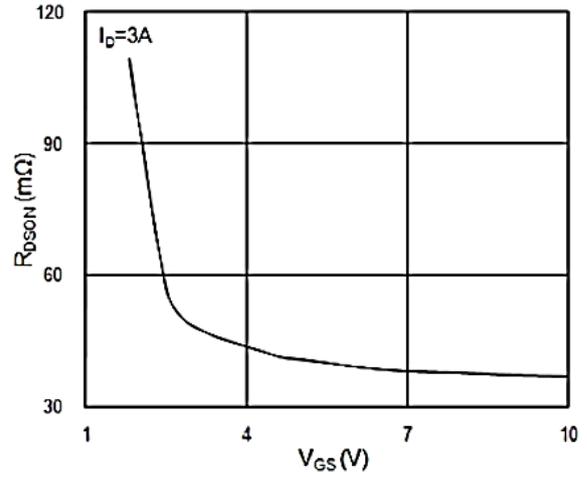


Fig.2 On-Resistance vs. G-S Voltage

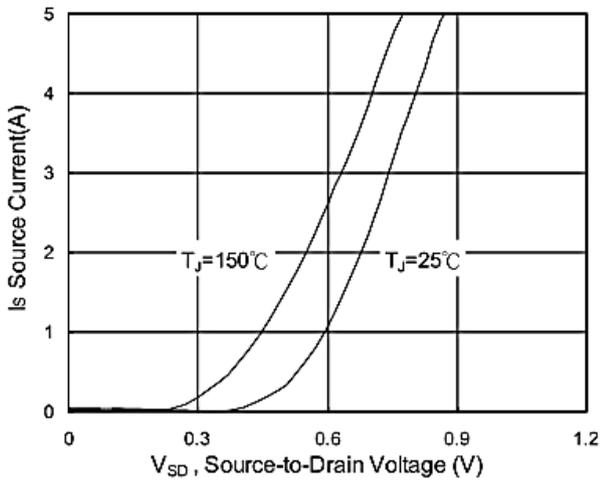


Fig.3 Source Drain Forward Characteristics

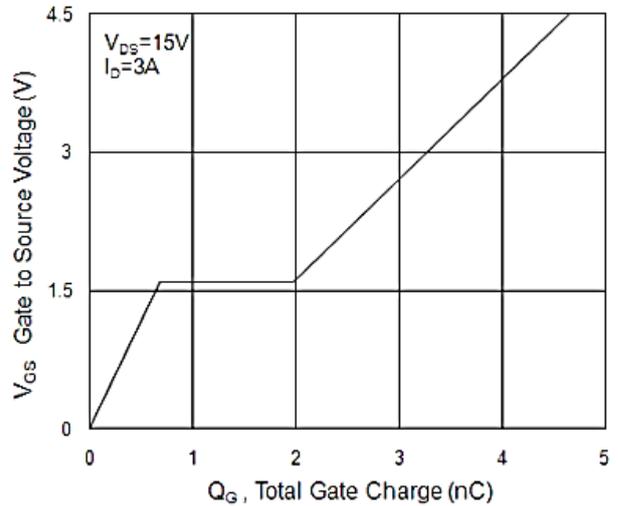


Fig.4 Gate-Charge Characteristics

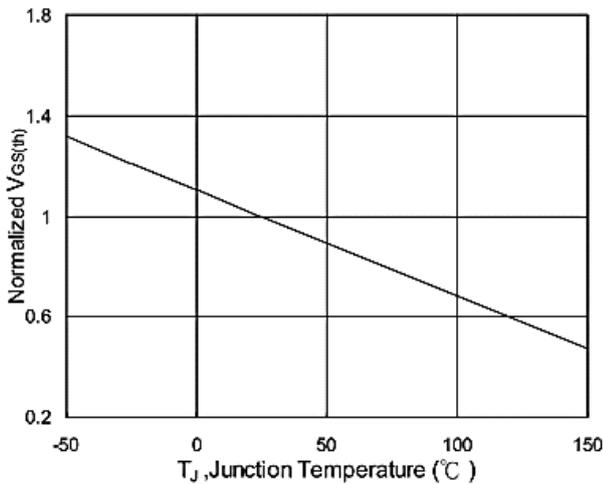


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

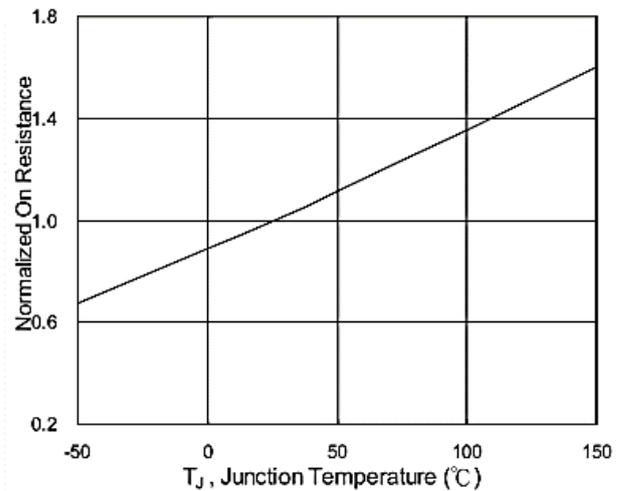


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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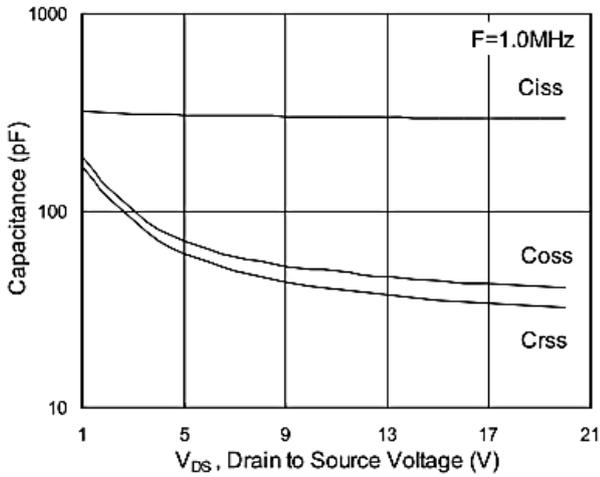


Fig.7 Capacitance

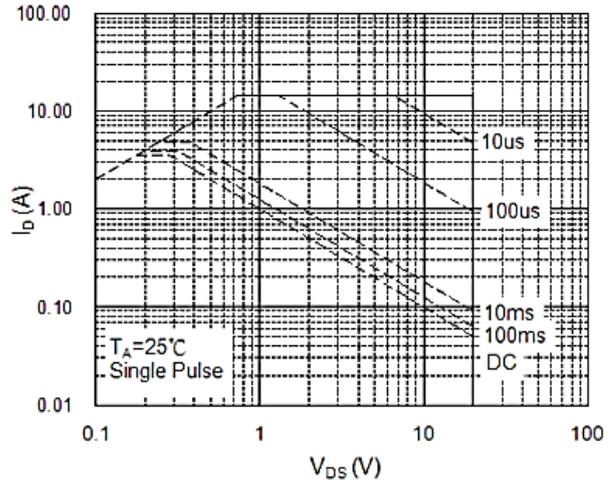


Fig.8 Safe Operating Area

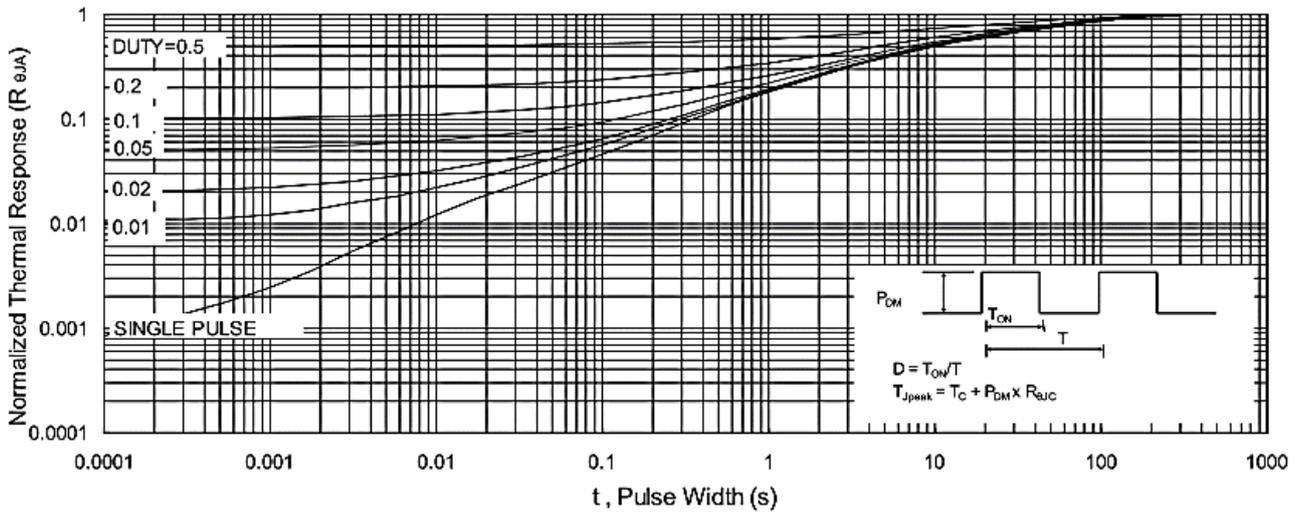


Fig.9 Normalized Maximum Transient Thermal Impedance

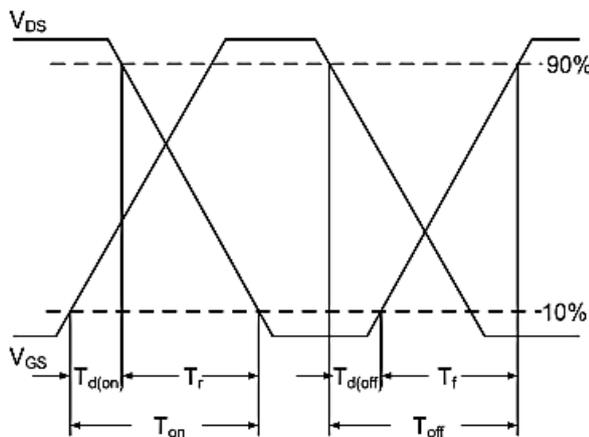


Fig.10 Switching Time Waveform

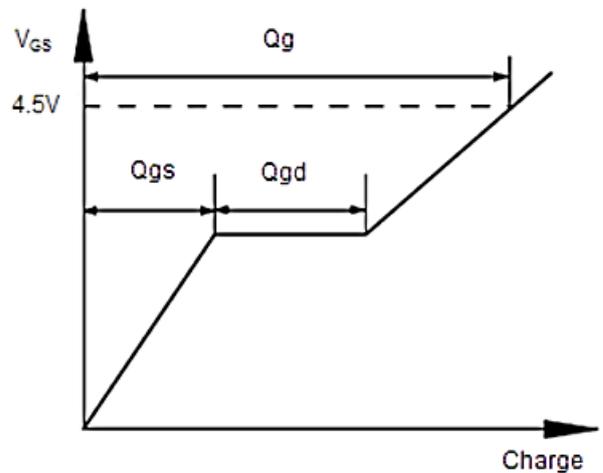


Fig.11 Gate Charge Waveform

P-Channel Typical Characteristics

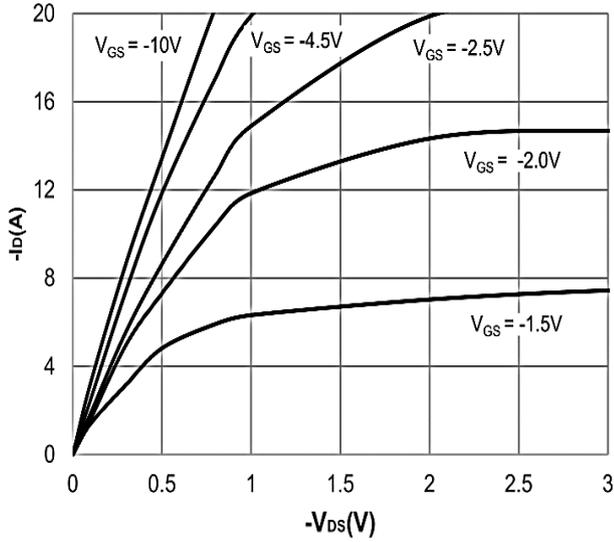


Figure 1: Output Characteristics

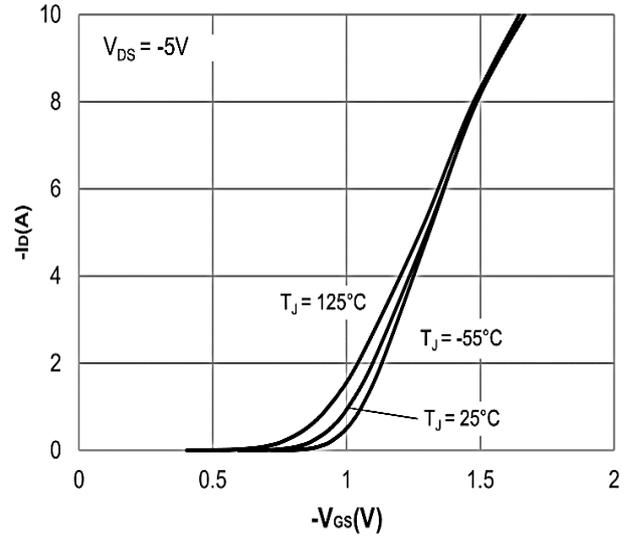


Figure 2: Typical Transfer Characteristics

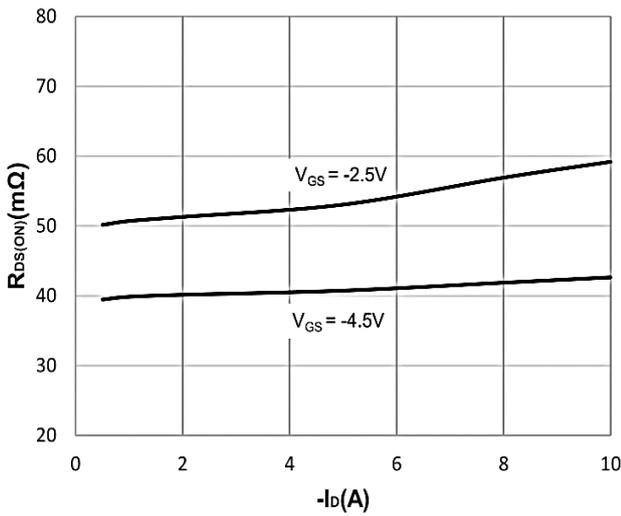


Figure 3: On-resistance vs. Drain Current

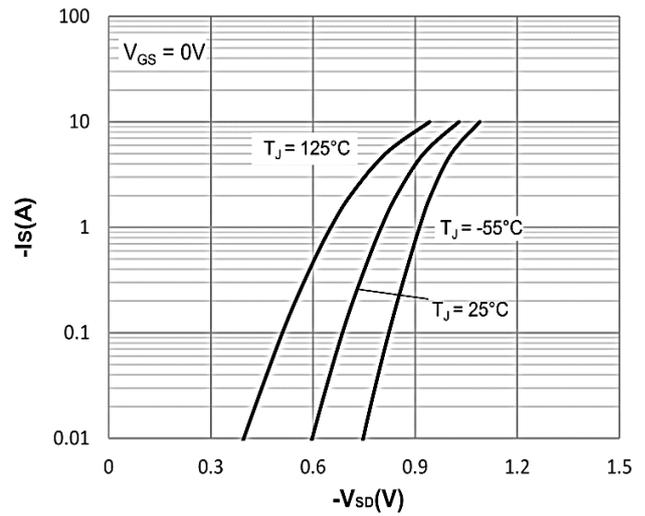


Figure 4: Body Diode Characteristics

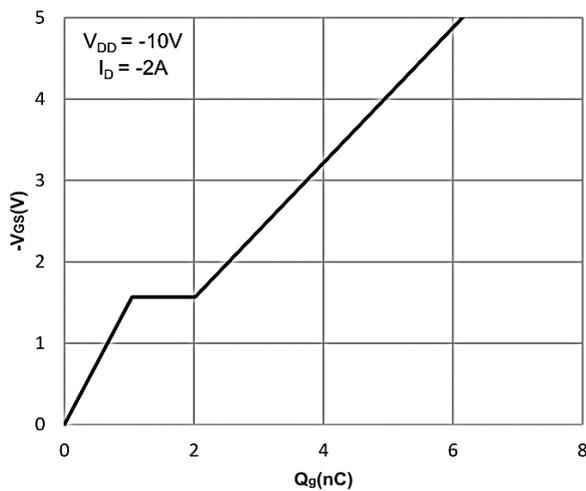


Figure 5: Gate Charge Characteristics

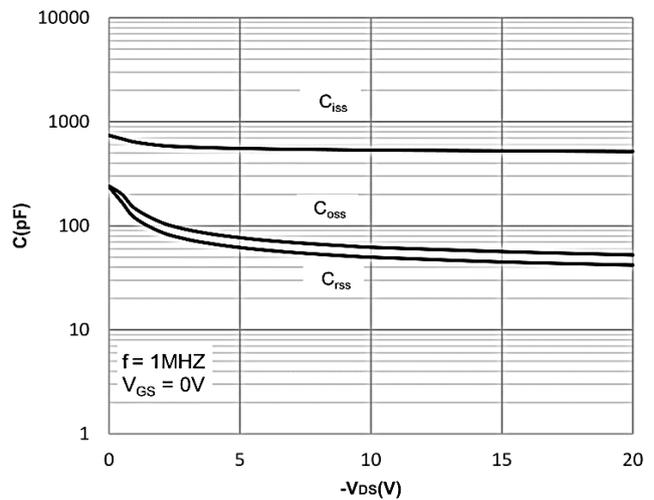


Figure 6: Capacitance Characteristics

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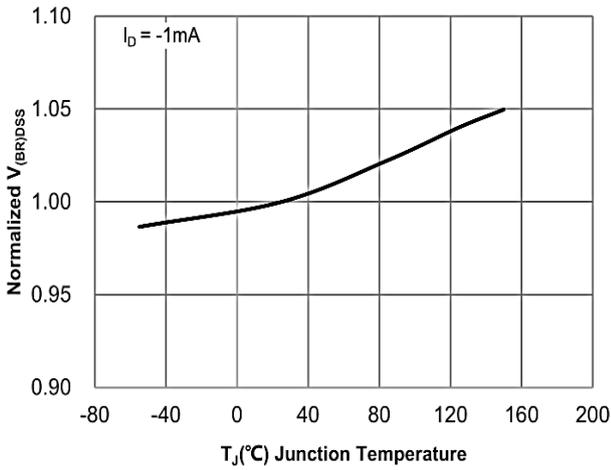


Figure 7: Normalized Breakdown voltage vs. Junction Temperature

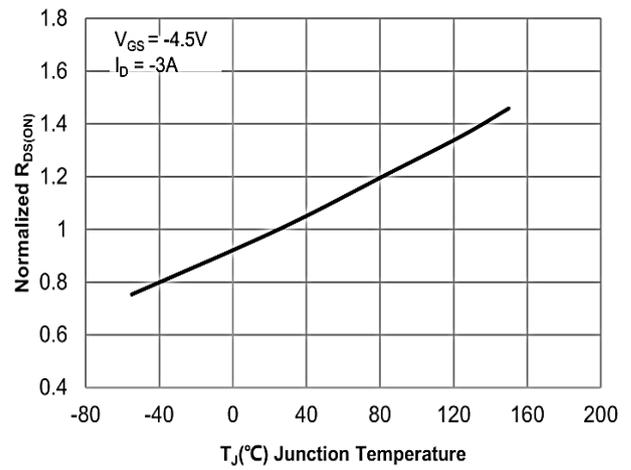


Figure 8: Normalized on Resistance vs. Junction Temperature

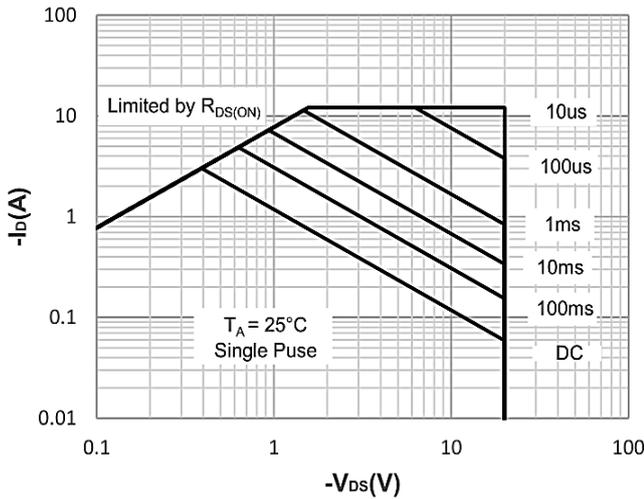


Figure 9: Maximum Safe Operating Area

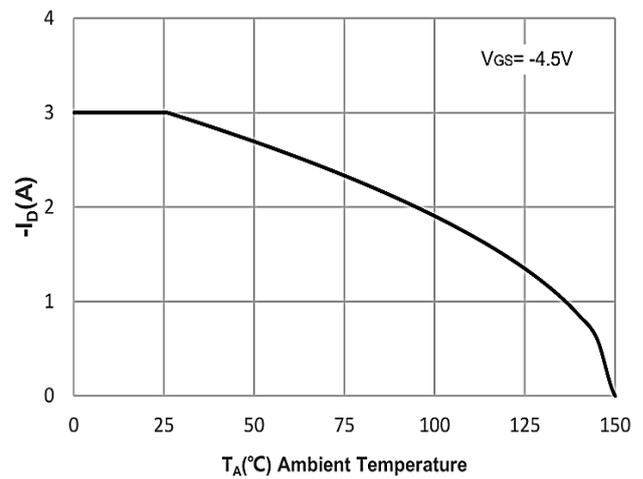


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

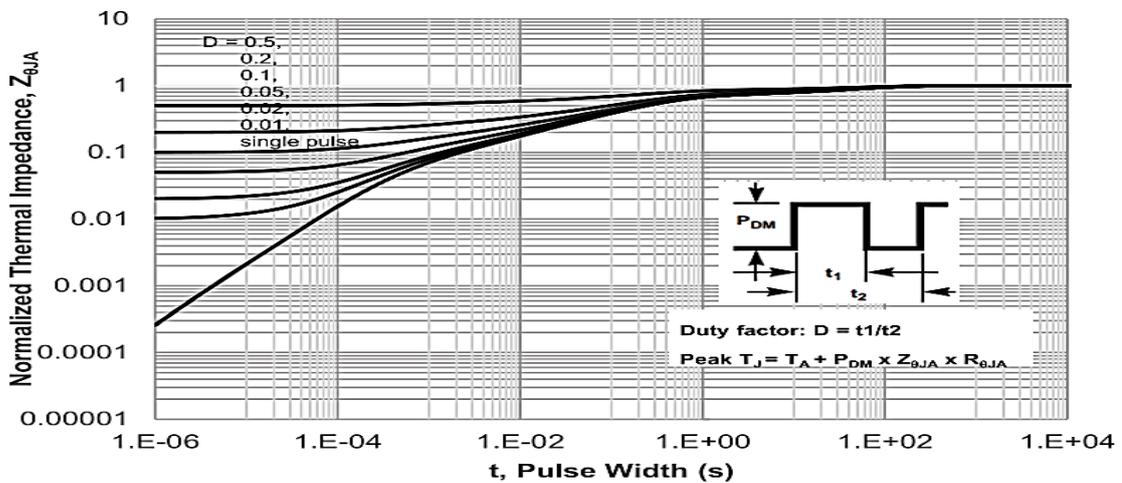
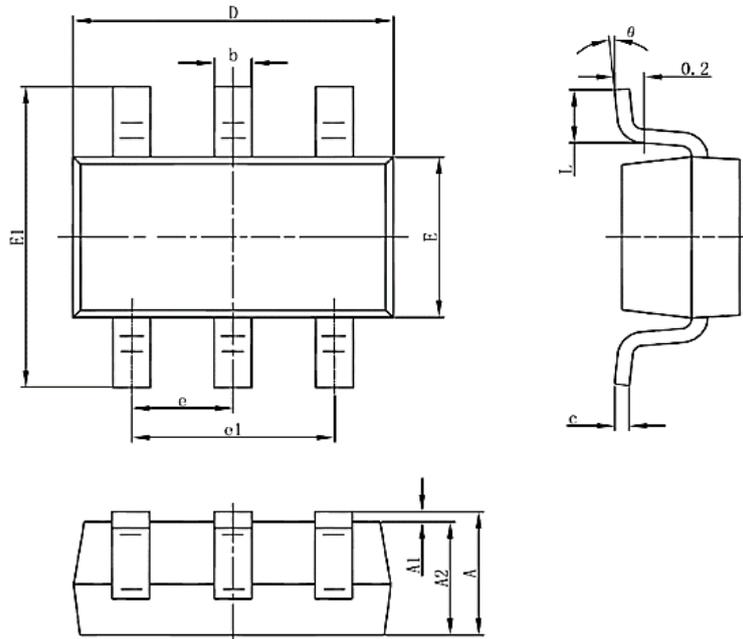


Figure 11: Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOT23-6-Double


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0	8	0	8

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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20V N+P-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2022/9/21	Initial release

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