

20V N+N-Channel Enhancement Mode MOSFET

Description

The AP8205S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

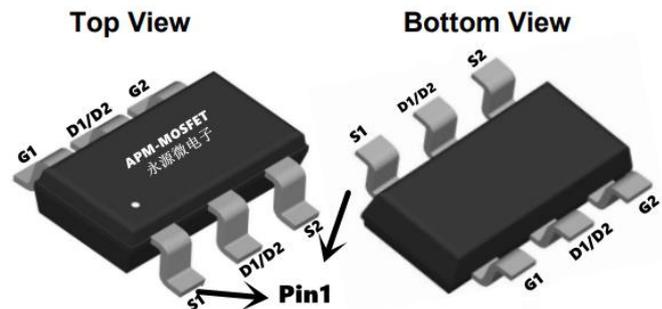
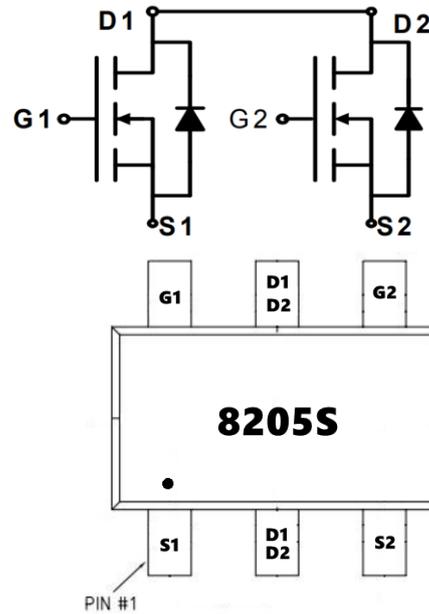
$V_{DS}=20V$ $I_D=6.5A$

$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=10V$ (Type: 21m Ω)

Application

Lithium battery protection

Mobile phone fast charging



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8205S	SOT23-6L	8205S	3000

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	20	V
VGS	Gate-Source Voltage	± 12	V
$I_{D@T_A=25^\circ C}$	Continuous Drain Current ¹	6.5	A
$I_{D@T_A=70^\circ C}$	Continuous Drain Current ¹	4.8	A
IDM	Pulsed Drain Current ²	24	A
$PD@T_A=25^\circ C$	Total Power Dissipation ³	1.5	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
TJ	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	85	$^\circ C/W$

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Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	22	---	V
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=5A$		21	25	mΩ
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=2.5V, I_D=4A$		28	40	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.5	0.7	1.2	V
IDSS	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 8V, V_{DS}=0V$	---	---	±100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=3.5A$	---	20	---	S
Qg	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=7A$	---	11.4	---	nC
Qgs	Gate-Source Charge		---	1.6	---	
Qgd	Gate-Drain Charge		---	2.9	---	
Td(on)	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3, I_D=5A$	---	5	---	ns
Tr	Rise Time		---	32.4	---	
Td(off)	Turn-Off Delay Time		---	28	---	
Tf	Fall Time		---	9	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	863	---	pF
Coss	Output Capacitance		---	87	---	
Crss	Reverse Transfer Capacitance		---	71	---	
Is	Continuous Source Current ^{1,4}	$V_G=V_D=0V, \text{Force Current}$	---	---	6	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\cong 300\mu s$, duty cycle $\cong 2\%$
- 4、The power dissipation is limited by 175°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics

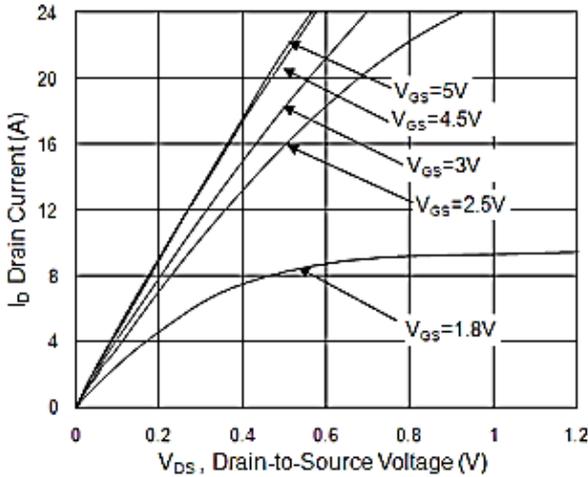


Fig.1 Typical Output Characteristics

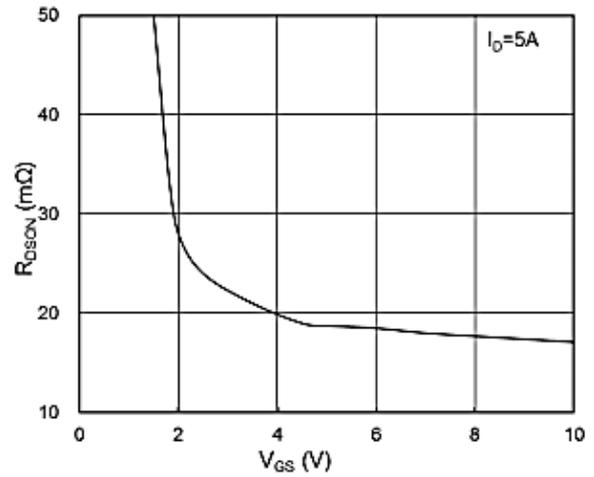


Fig.2 On-Resistance vs. Gate-Source Voltage

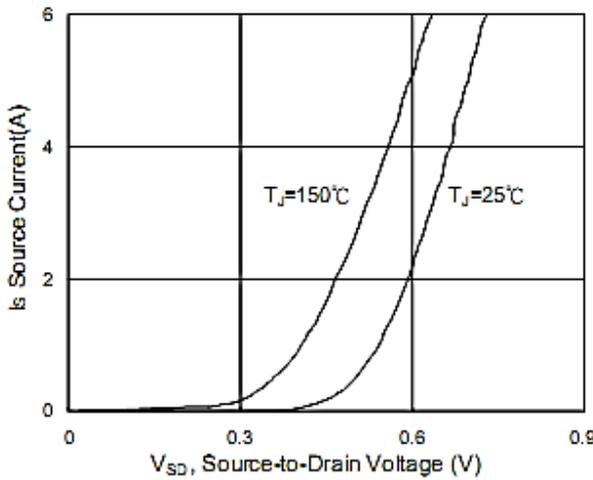


Fig.3 Forward Characteristics of Reverse

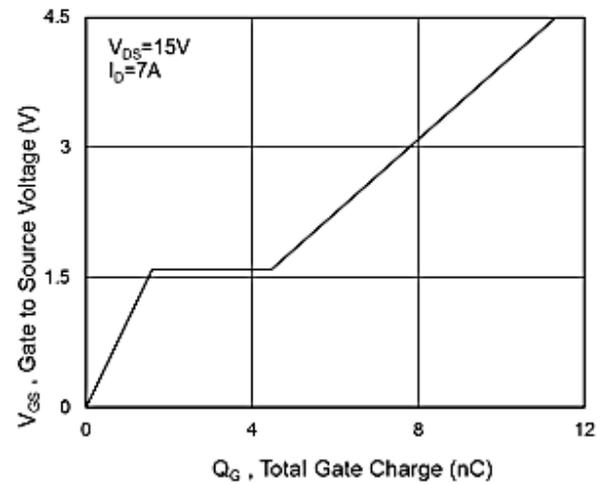


Fig.4 Gate-Charge Characteristics

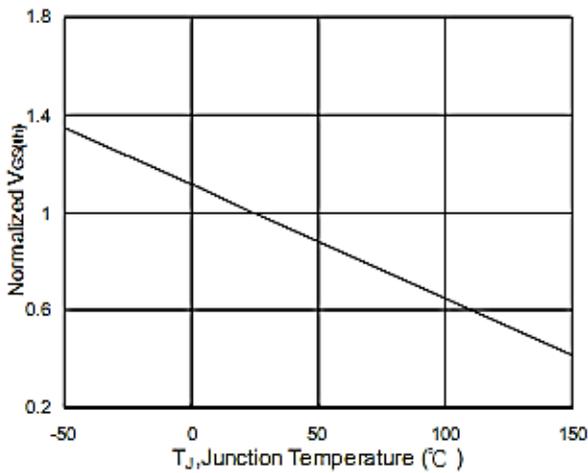


Fig.5 $V_{GS(th)}$ vs. T_J

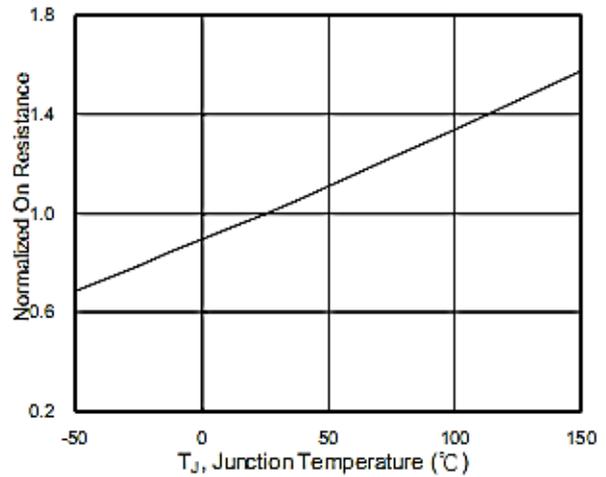


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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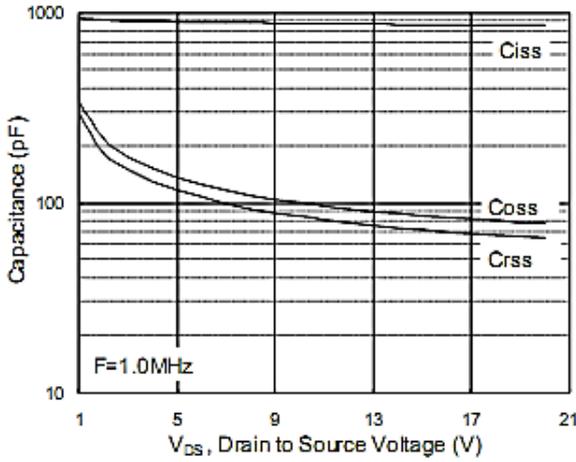


Fig.7 Capacitance

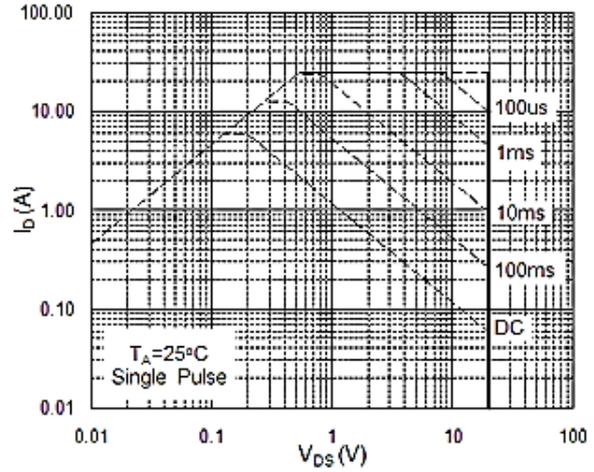


Fig.8 Safe Operating Area

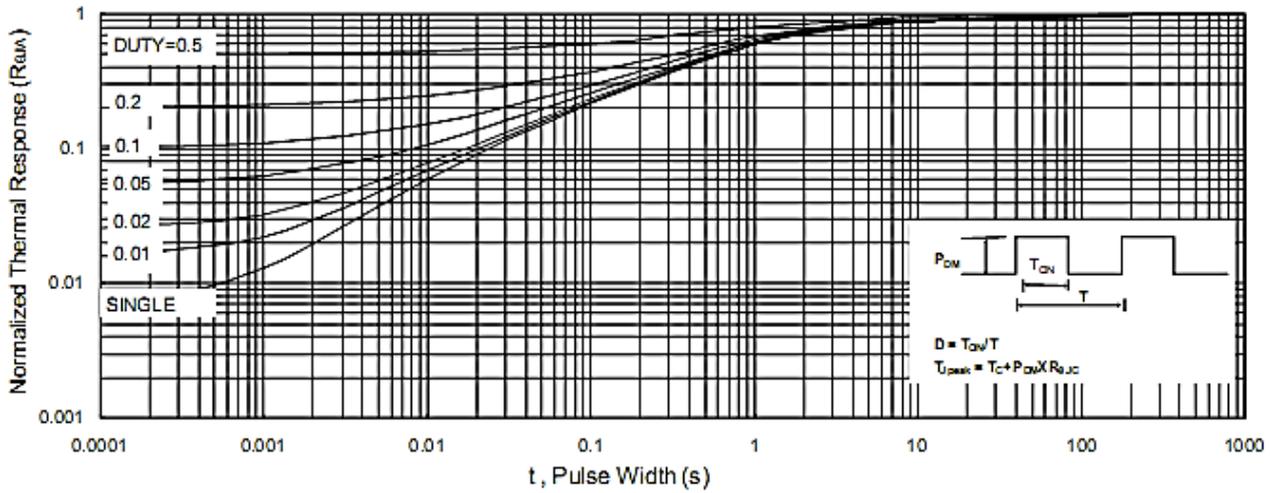


Fig.9 Normalized Maximum Transient Thermal Impedance

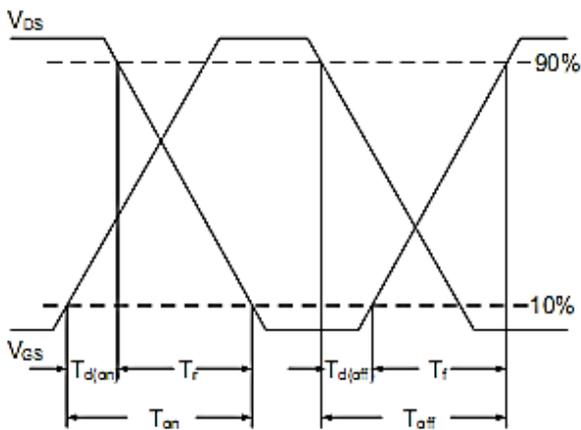


Fig.10 Switching Time Waveform

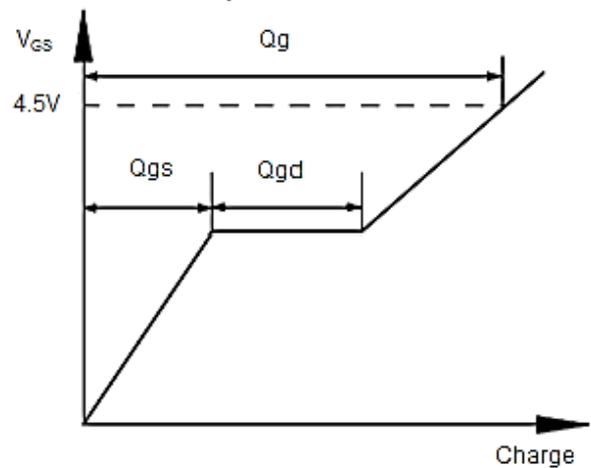
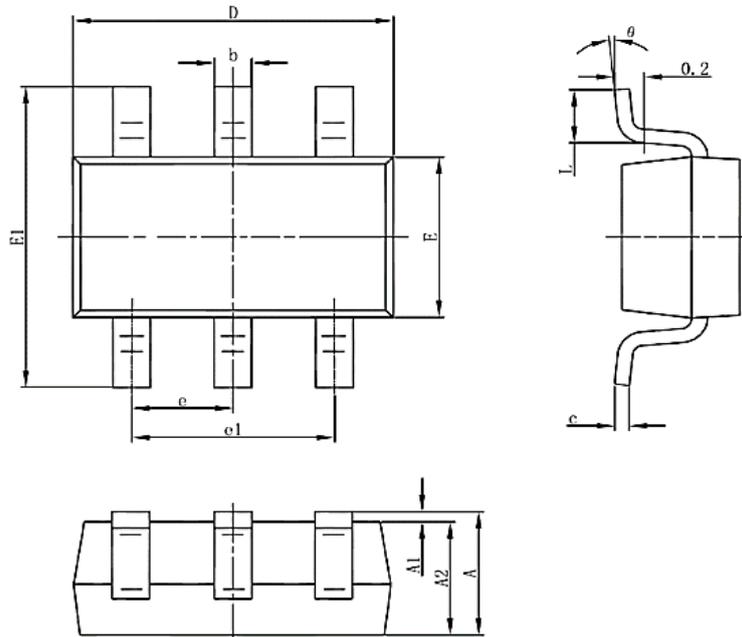


Fig.11 Gate Charge Waveform

Package Mechanical Data-SOT23-6-Single


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0	8	0	8

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Edition	Date	Change
Rve3.8	2018/1/31	Initial release
Rve3.9	2021/12/10	Change layout format

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