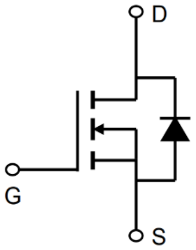
60V N-Channel Enhancement Mode MOSFET



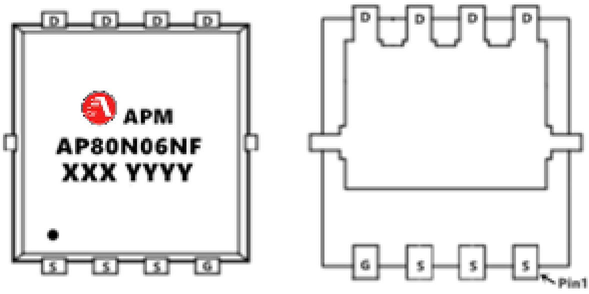
Description

The AP80N06NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 60V I_D =80A

$R_{DS(ON)}$ < 6.0mΩ @ V_{GS}=10V **（Type：4.5mΩ）**

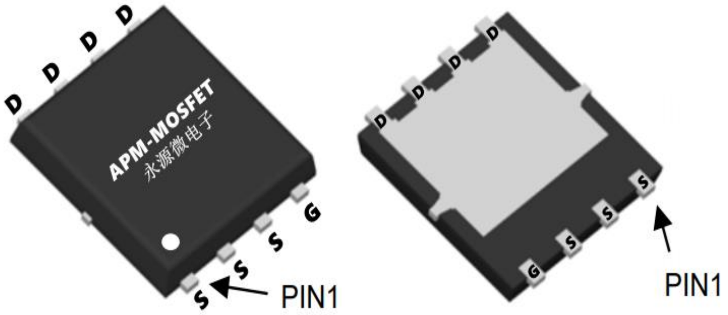


Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N06NF	PDN5*6-8L	AP80N06NF XXX YYYY	5000PCS

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Value	Unit
VDS	Drain source voltage	60	V
VGS	Gate source voltage	±20	V
I_D@T_C=25℃	Continuous drain current$^{1)}$	80	A
I_D@T_C=100℃	Continuous drain current$^{1)}$	45	A
IDM	Pulsed drain current$^{2)}$	210	A
IAS	Diode forward current	70	A
P_D@T_C=25℃	Power dissipation	87	W
EAS	Single pulsed avalanche energy$^{)}$	66	mJ
Tstg，Tj	Operation and storage temperature	-55 to 150	℃
RθJC	Thermal resistance, junction-case	1.44	℃/W
RθJA	Thermal resistance, junction-ambient$^{4)}$	62	℃/W

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
BVDSS	Drain-source breakdown voltage	V_{GS}=0 V, I_D=250 μA	60	72		V
VGS(th)	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250 μA	1.2	1.8	2.5	V
RDS(ON)	Drain-source on-state resistance	V_{GS}=10 V, I_D=20 A		4.5	6.0	mΩ
RDS(ON)	Drain-source on-state resistance	V_{GS}=4.5 V, I_D=10 A		6.4	10	mΩ
IGSS	Gate-source leakage current	V_{GS}=±20 V			±100	nA
IDSS	Drain-source leakage current	V_{DS}=60 V, V_{GS}=0 V			1	μA
Rg	Gate Resistance	f=1MHz		2.8		Ω
Ciss	Input capacitance	V_{GS}=0 V, V_{DS}=50 V, ƒ=100 kHz		2136		pF
Coss	Output capacitance			331.5		pF
Crss	Reverse transfer capacitance			10.6		pF
td(on)	Turn-on delay time	V_{GS}=10 V, V_{DS}=50 V, R_G=2 Ω, I_D=25 A		22.9		ns
t_r	Rise time			6.5		ns
td(off)	Turn-off delay time			45.7		ns
t_f	Fall time			20.4		ns
Q_g	Total gate charge	I_D=25 A, V_{DS}=50 V, V_{GS}=10 V		30		nC
Q_{gs}	Gate-source charge			5.8		nC
Qgd	Gate-drain charge			6.1		nC
Vplateau	Gate plateau voltage			3.6		V
VSD	Diode forward voltage	I_S=20 A, V_{GS}=0 V			1.3	V
trr	Reverse recovery time	I_S=25A, di/dt=100 A/μs		50.3		ns
Q_{rr}	Reverse recovery charge			45.1		nC
Irrm	Peak reverse recovery current			1.5		A

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .

3、The power dissipation is limited by 175℃ junction temperature

4、EAS condition: TJ=25℃, V_{DD}=25V,V_{GS}=10V,L=0.1Mh,I_{AS}=40A

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

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Typical Characteristics

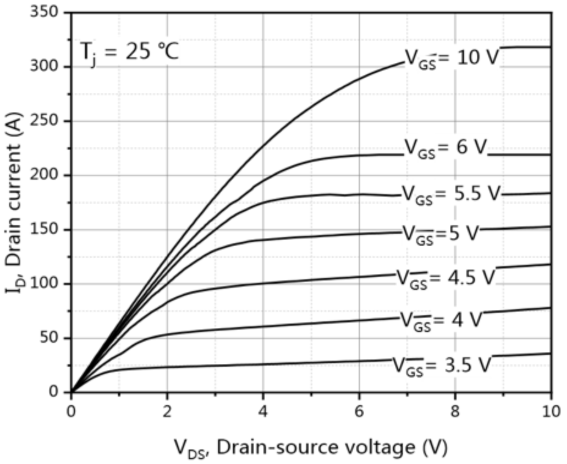

Figure1.Type Output Charcteristics

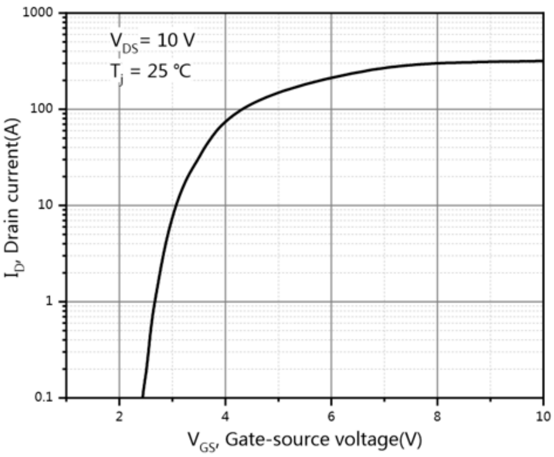

Figure2.Type Transfer Charcteristics

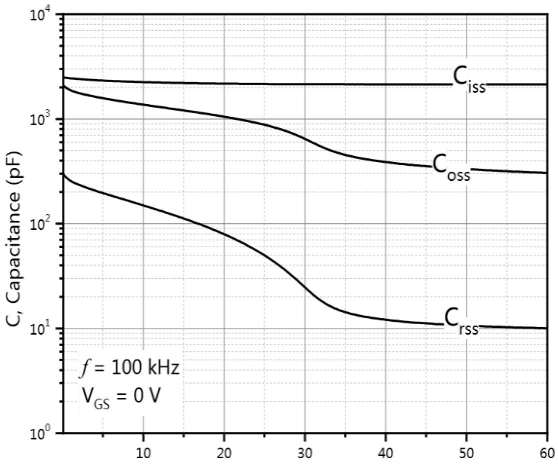

Figure3.Typ Capacitances

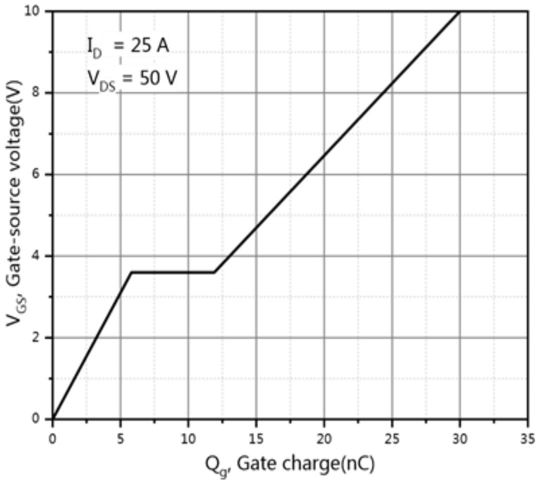

Figure4.Typ Gate Charge

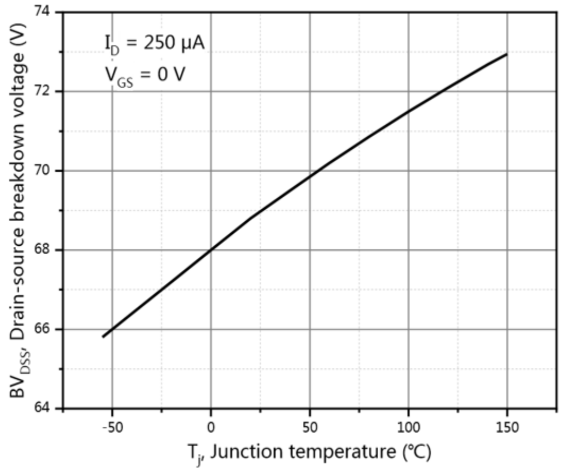

Figure5.Drain-source Breakdown Voltage

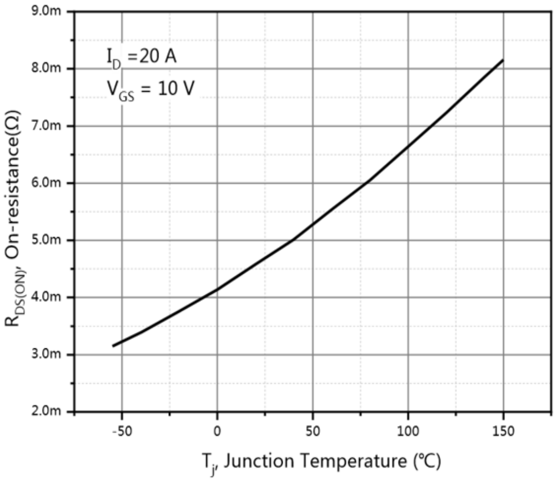

Figure6.Drain-source on-state resistance

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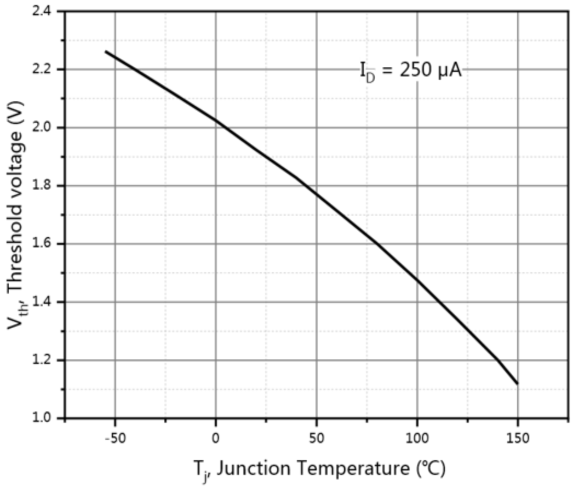


Figure7.Threshold Voltage

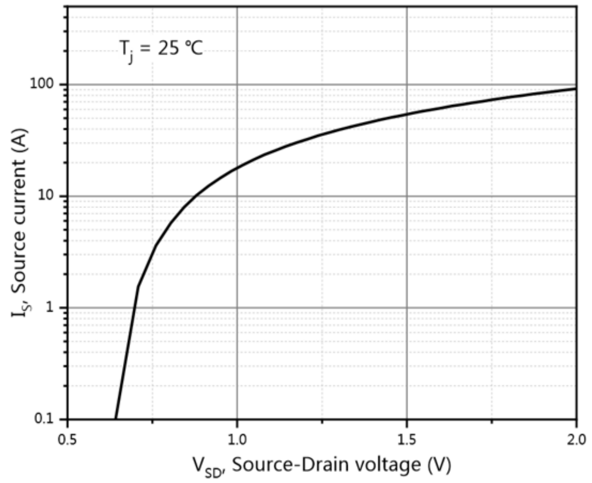


Figure8.Forward characteristic of body diode

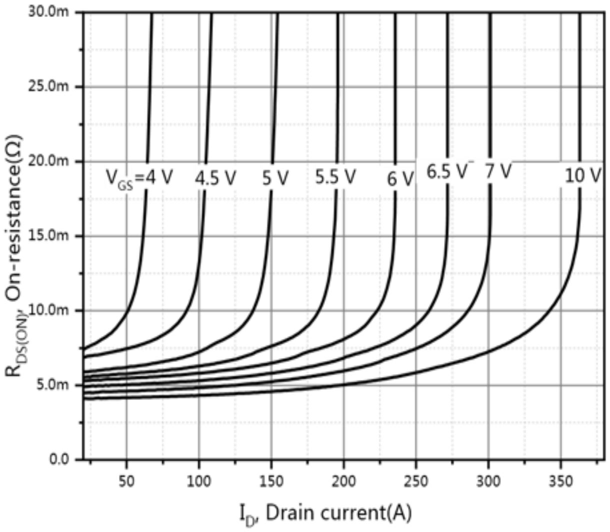


Figure9.Drani-source on-state resistance

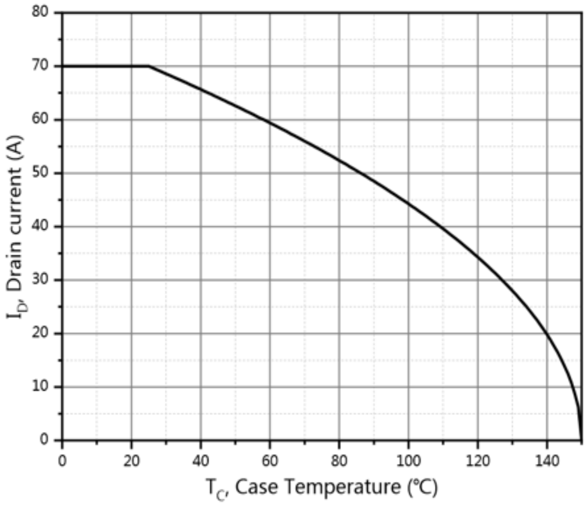


Figure10.Drain-current

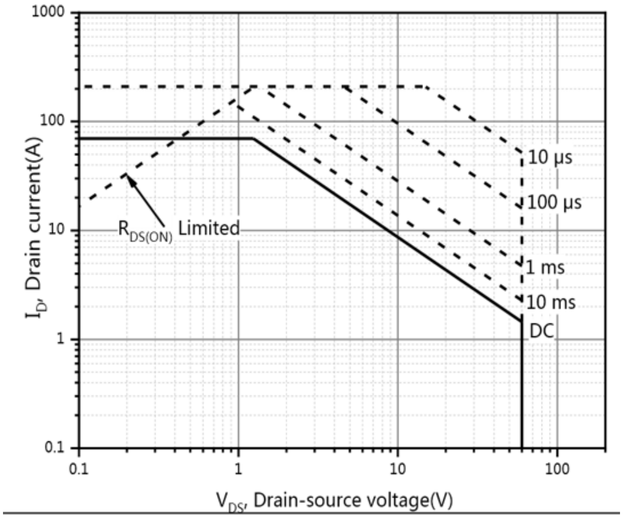


Figure11.Safe operation area fo Tc=25℃

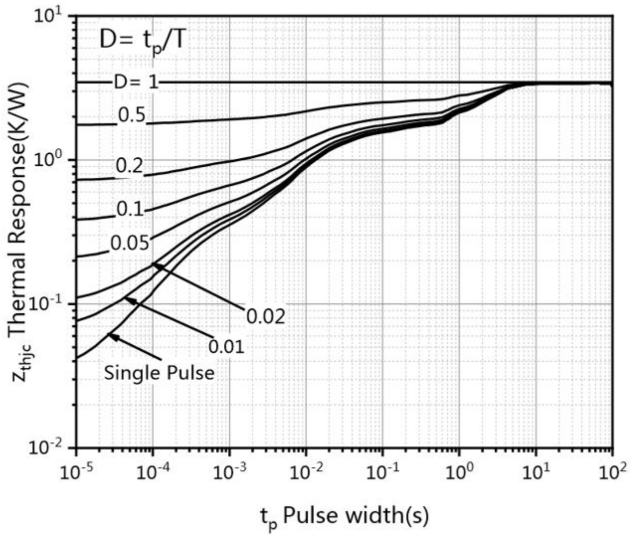
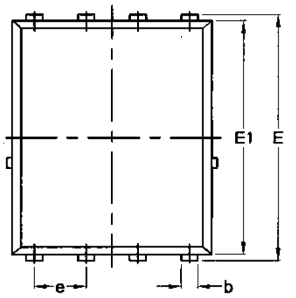
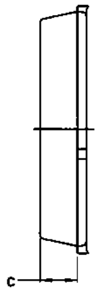
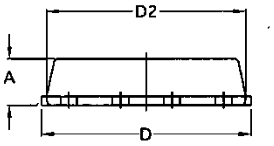


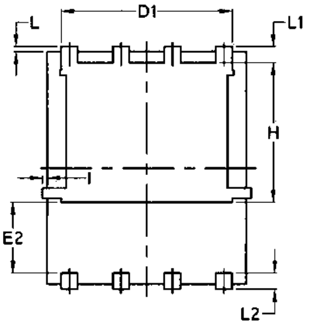
Figure12.Safe operation area fo PDFN5*6-8L

Package Mechanical Data-PDFN5*6-8L Single



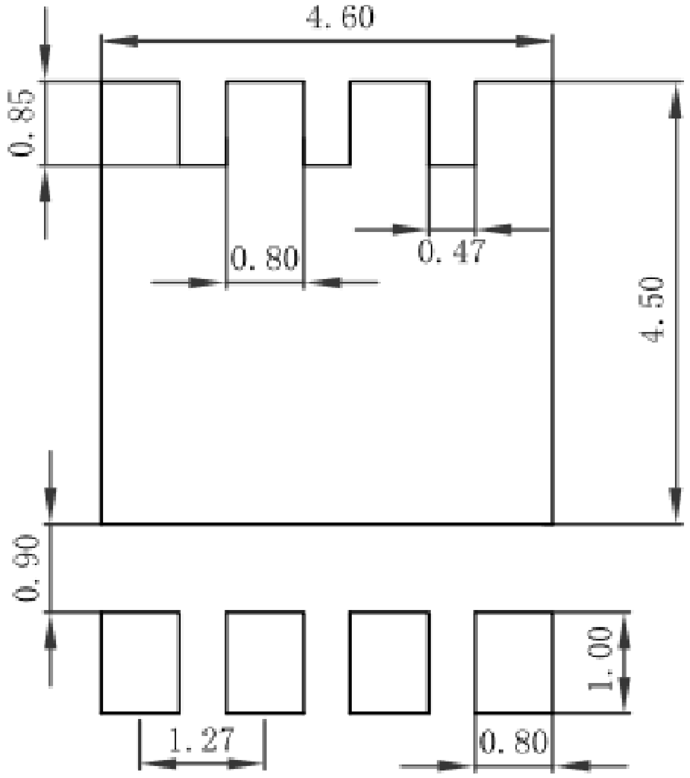






Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

PCB LAYOUT



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Edition	Date	Change
REV1.0	2019/8/1	Initial release
REV1.1	2023/9/7	Reduce Rds
REV1.2	2023/4/14	Update LOGO And Increase PCB Layout