

## 30V N-Channel Enhancement Mode MOSFET

### Description

The AP80N03D uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS}=30V$   $I_D=80A$

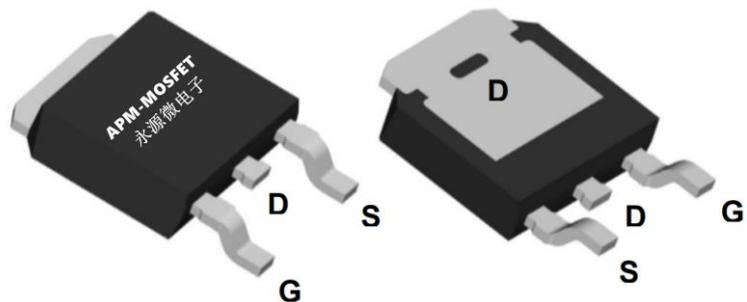
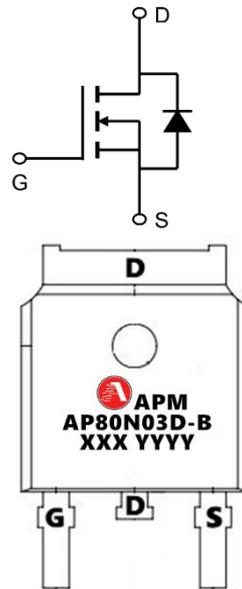
$R_{DS(ON)} < 5.5m\Omega @ V_{GS}=10V$  (Type: 4.0m $\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N03D	TO-252-3L	AP80N03D XXXX YYYY	2500

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	80	A
$I_D@T_C=75^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	50	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	240	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	56	mJ
$I_{AS}$	Avalanche Current	15	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	46	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	2.72	W
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.72	$^\circ\text{C/W}$

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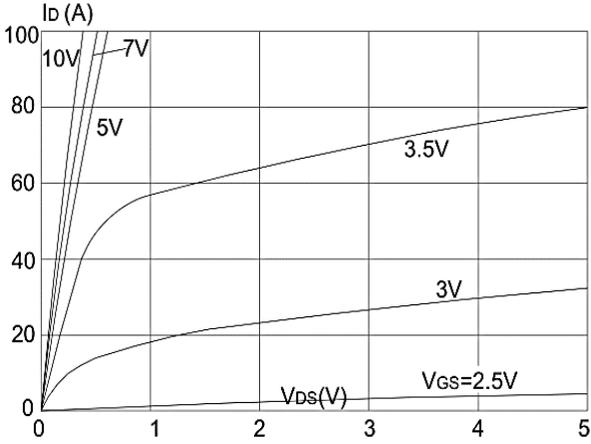
### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	32	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> = 0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0	1.6	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	4.0	5.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	6.1	8.5	
Ciss	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f = 1.0MHz	-	1614	-	pF
Coss	Output Capacitance		-	245	-	pF
Crss	Reverse Transfer Capacitance		-	215	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =30A, V <sub>GS</sub> =10V	-	33.7	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	8.5	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	7.5	-	nC
td(on)	Turn-on Delay Time	V <sub>DS</sub> =15V, I <sub>D</sub> =30A, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =10V	-	7.5	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	14.5	-	ns
td(off)	Turn-off Delay Time		-	35.2	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	9.6	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	70	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	280	A
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> =30A	-	-	1.2	V

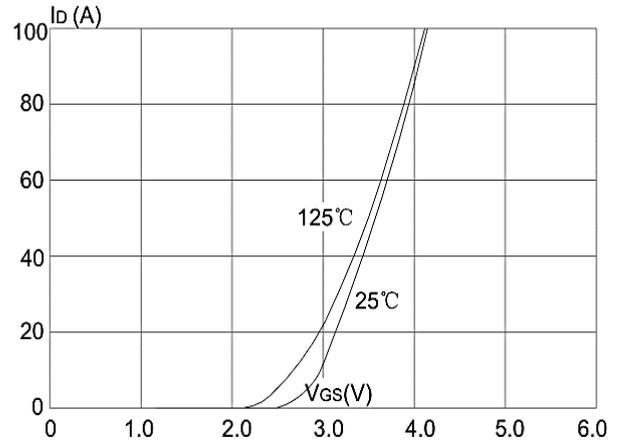
**Note :**

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The EAS data shows Max. rating . The test condition is VDD=24V, VGS=10V, L=0.5mH, IAS=18A
- 4、 The power dissipation is limited by 175°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

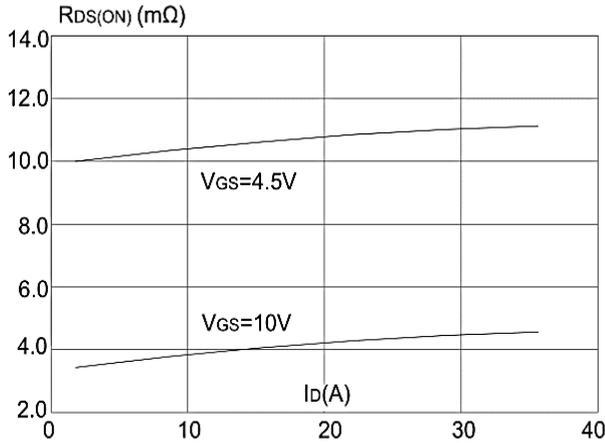
**Typical Characteristics**



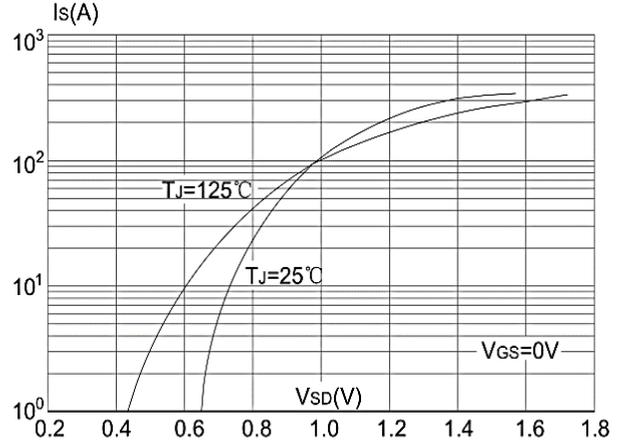
**Figure 1: Output Characteristics**



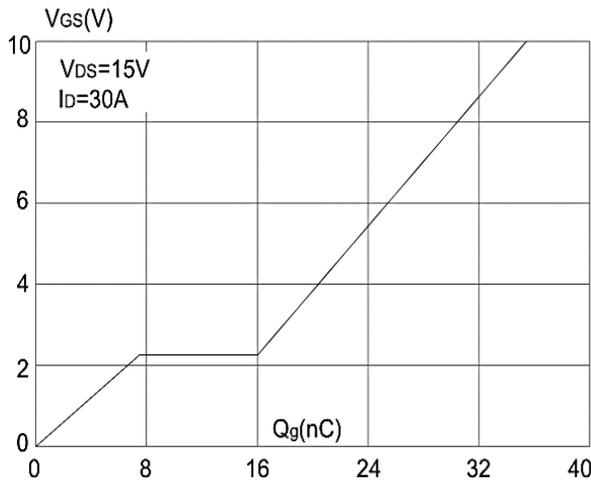
**Figure 2: Typical Transfer Characteristics**



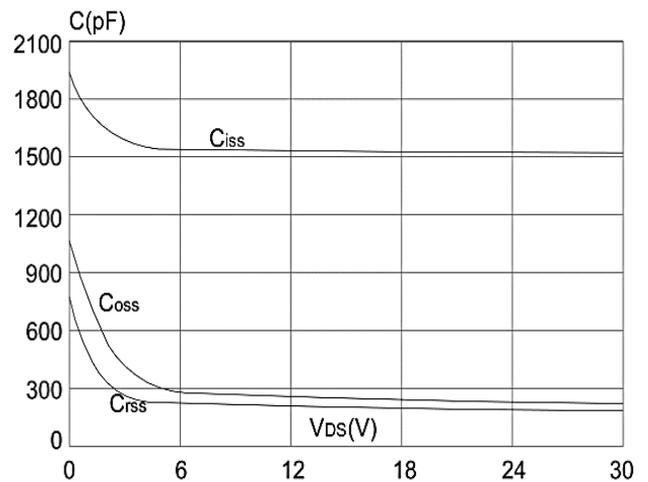
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**

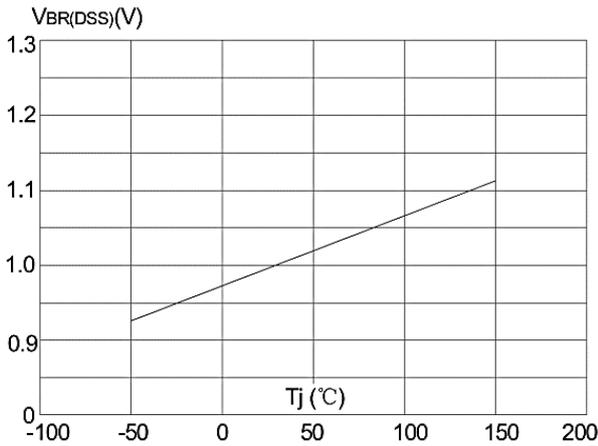


**Figure 5: Gate Charge Characteristics**

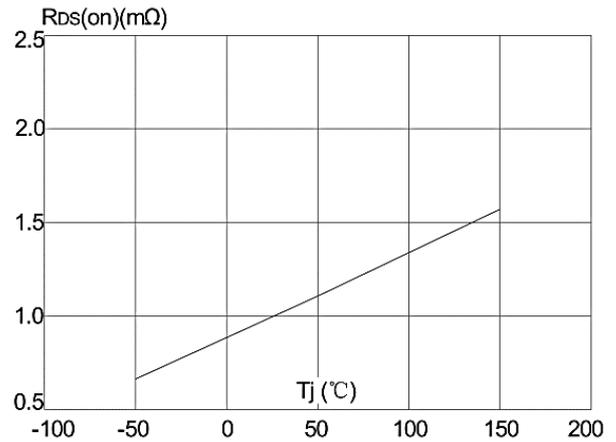


**Figure 6: Capacitance Characteristics**

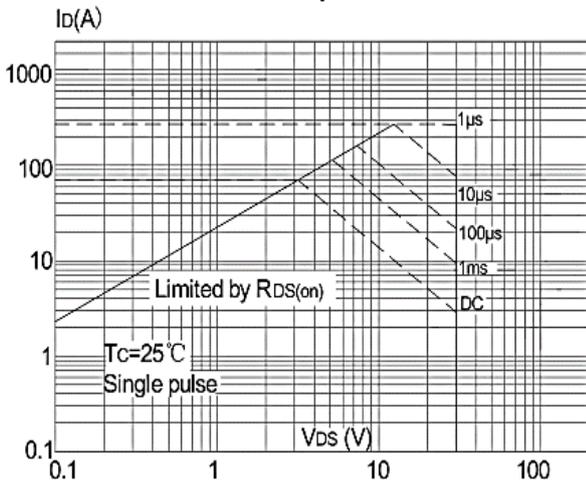
**30V N-Channel Enhancement Mode MOSFET**



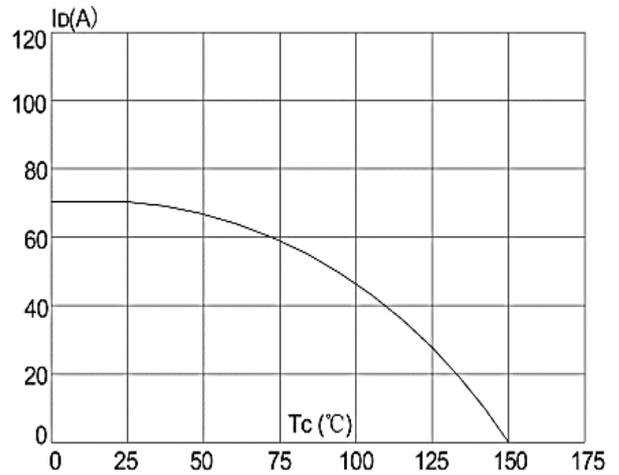
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



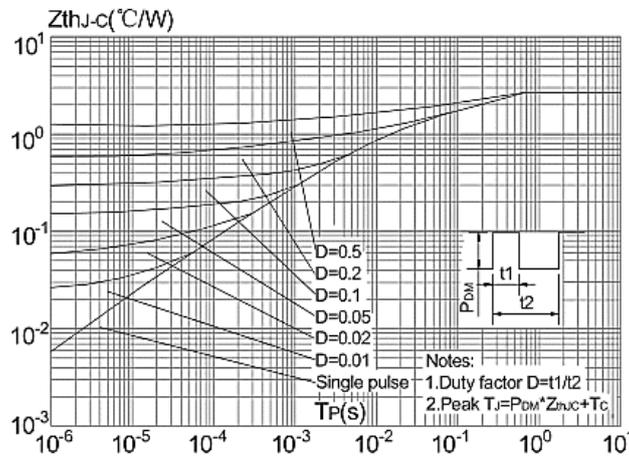
**Figure 8: Normalized on Resistance vs. Junction Temperature**



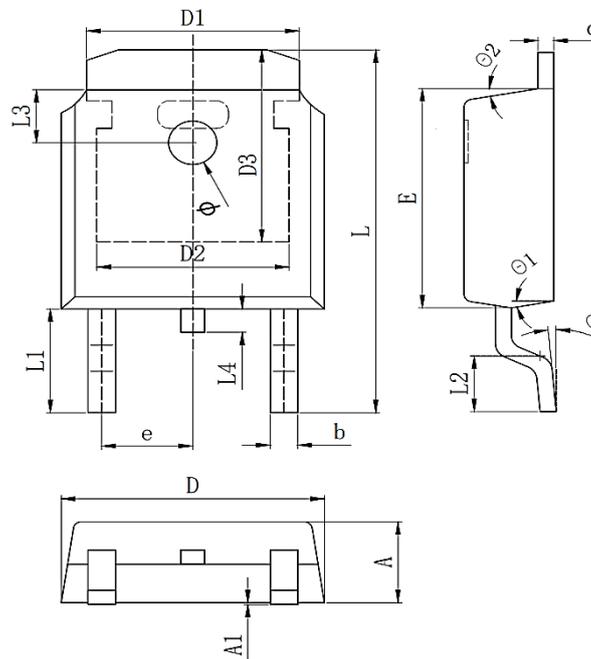
**Figure 9: Maximum Safe Operating Area vs. Case Temperature**



**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ca**

**Package Mechanical Data-TO-252-3L**


Symbol	Dim in mm		
	Min	Typ	Max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.64	0.75	0.86
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	4.83REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	2.286TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
$\phi$	1.1	1.2	1.3
$\theta$	0°		10°
$\theta_1$	5°		10°
$\theta_2$	5°		10°

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Edition	Date	Change
REV1.0	2025/5/1	Initial release

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