

## 30V N-Channel Enhancement Mode MOSFET

### Description

The AP75N03NF uses advanced **APM-SGT V** technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 30V$   $I_D = 75A$

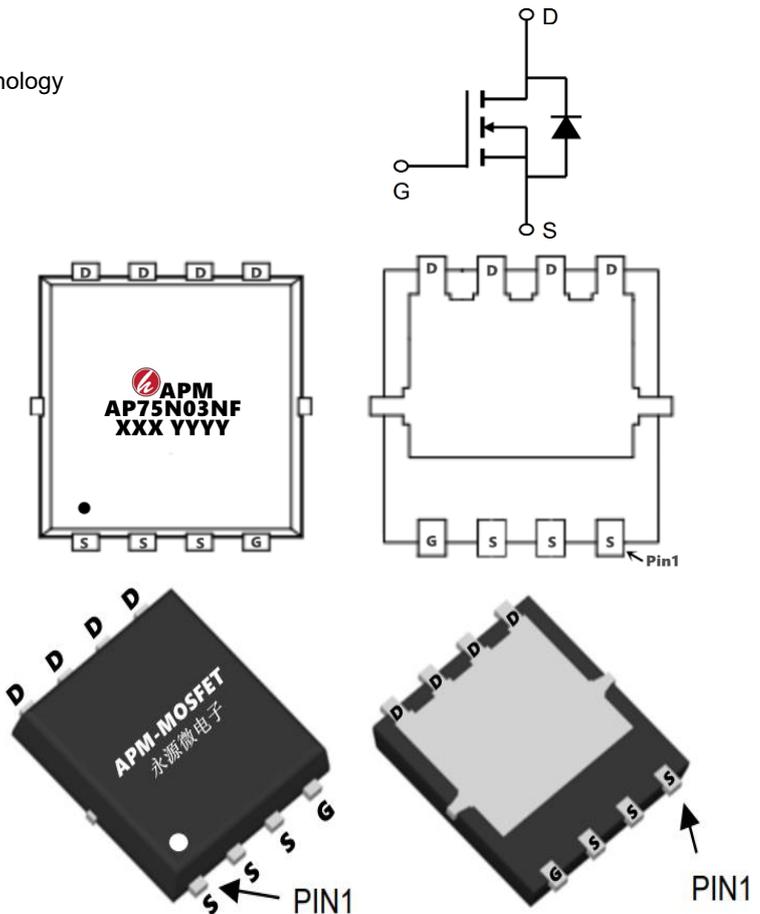
$R_{DS(ON)} < 5.8m\Omega @ V_{GS}=10V$  (Type: **3.5m $\Omega$** )

**$C_{iss} \approx 1010 PF$**

### Application

Buck

Boost



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP75N03NF	PDFN5*6-8L	AP75N03NF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_{D@TC=25^\circ C}$	Continuous Drain Current, $V_{GS} @ 10V_1$	75	A
$I_{D@TC=100^\circ C}$	Continuous Drain Current, $V_{GS} @ 10V_1$	32	A
$I_{DM}$	Pulsed Drain Current	300	A
$E_{AS}$	Single Pulsed Avalanche Energy	28.8	mJ
$I_{AS}$	Avalanche Current	24	A
$PD@TC=25^\circ C$	Power Dissipation	24	W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	25	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.2	$^\circ C/W$
$T_J$ TSTG	Operating Junction Temperature Range	-55 to 150	$^\circ C$



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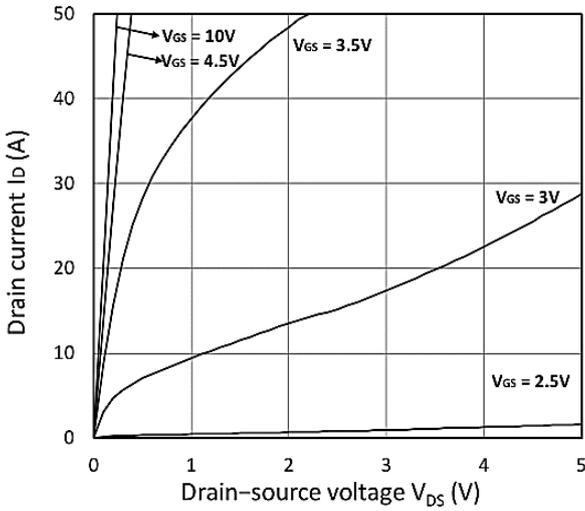
### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	30	-	-	V
IGSS	Gate-body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current T <sub>J</sub> =25°C	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V	-	-	1	μA
	Zero Gate Voltage Drain Current T <sub>J</sub> =100°C		-	-	100	
VGS(th)	Gate-Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.6	2.5	V
RDS(on)	Drain-Source On-Resistance <sup>4</sup>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	3.5	5.8	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	-	5.0	9.0	
gfs	Forward Transconductance <sup>4</sup>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A	-	70	-	S
Ciss	Input Capacitance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1MHz	-	1010	-	pF
Coss	Output Capacitance		-	420	-	
Crss	Reverse Transfer Capacitance		-	46	-	
R <sub>g</sub>	Gate Resistance	f = 1MHz	-	2.2	-	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 15V, I <sub>D</sub> = 20A	-	16	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	3	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	3.3	-	
td(on)	Turn-On Delay Time	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 15V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	6.3	-	ns
t <sub>r</sub>	Rise Time		-	3.2	-	
td(off)	Turn-Off Delay Time		-	18	-	
t <sub>f</sub>	Fall Time		-	3.6	-	
trr	Body Diode Reverse Recovery Time	I <sub>F</sub> = 20A, dI/dt = 100A/μs	-	10	-	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge		-	13.2	-	nC
VSD	Diode Forward Voltage <sup>4</sup>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V
IS	Continuous Source Current	T <sub>C</sub> = 25°C	-	-	50	A

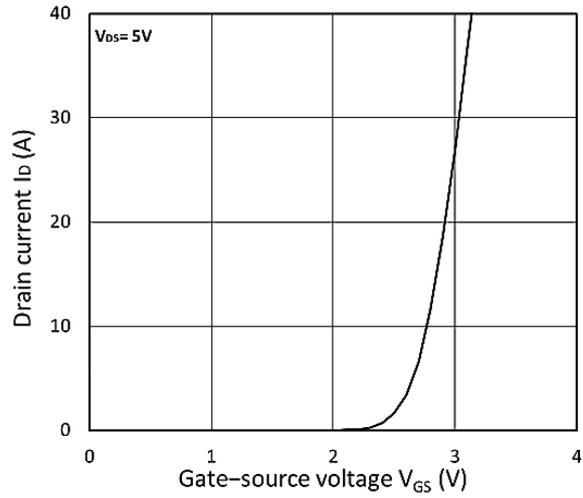
**Note :**

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%
- 3、 The EAS data shows Max. rating . The test condition is VDD =25V,VGS =10V,L=0.1mH,IAS =24A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

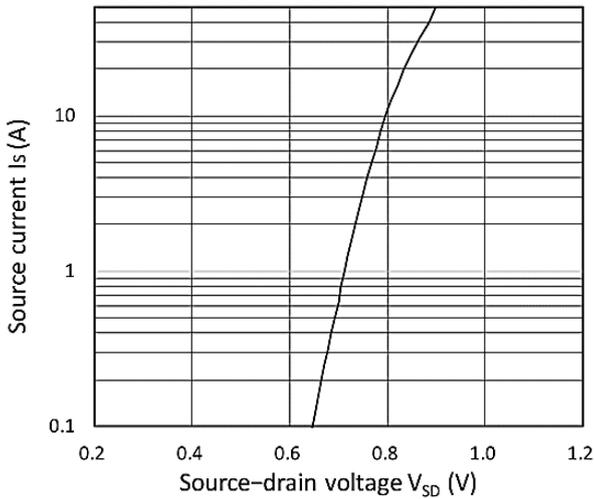
### Typical Characteristics



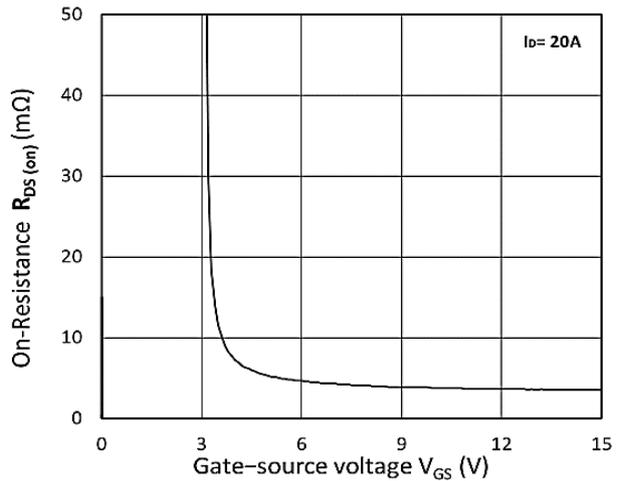
**Figure 1. Output Characteristics**



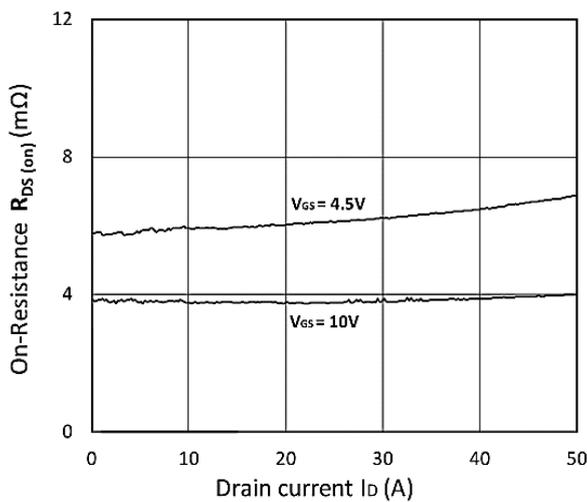
**Figure 2. Transfer Characteristics**



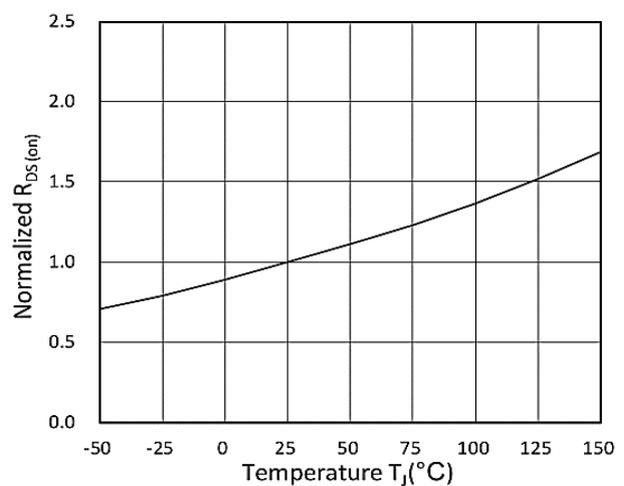
**Figure 3. Forward Characteristics of Reverse**



**Figure 4.  $R_{DS(ON)}$  vs.  $V_{GS}$**



**Figure 5.  $R_{DS(ON)}$  vs.  $I_D$**



**Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature**



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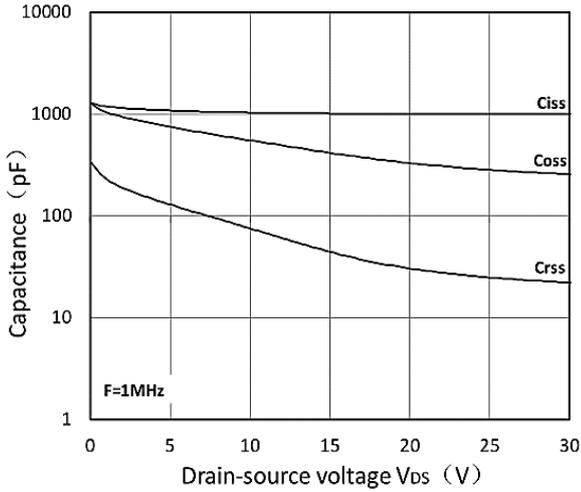


Figure 7. Capacitance Characteristics

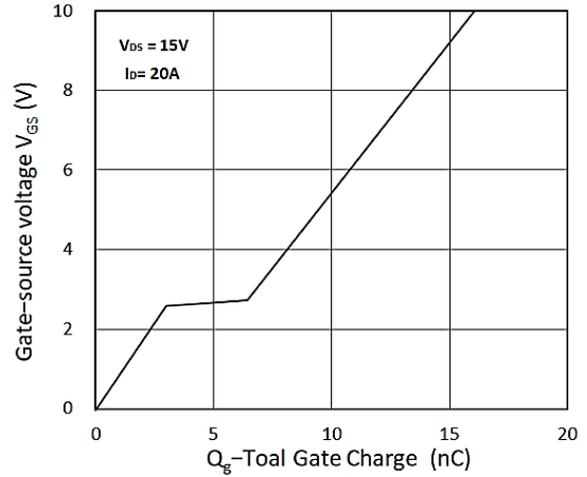


Figure 8. Gate Charge Characteristics

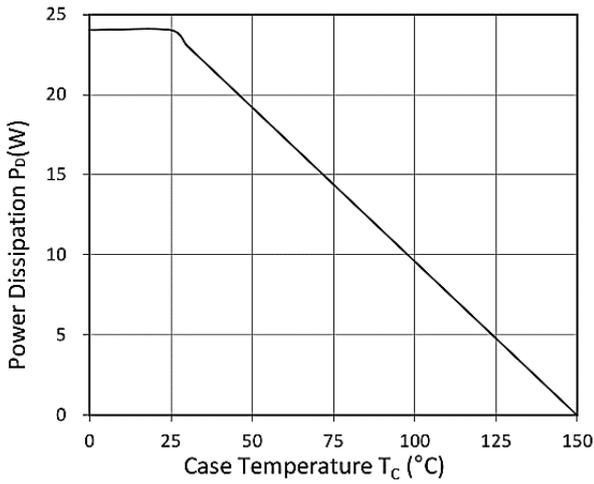


Figure 9. Power Dissipation

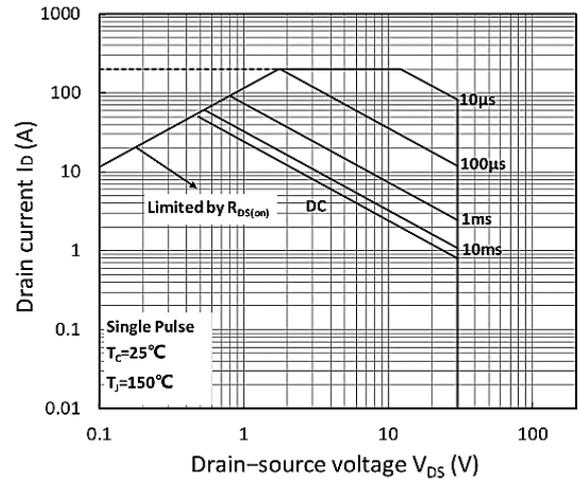


Figure 10. Safe Operating Area

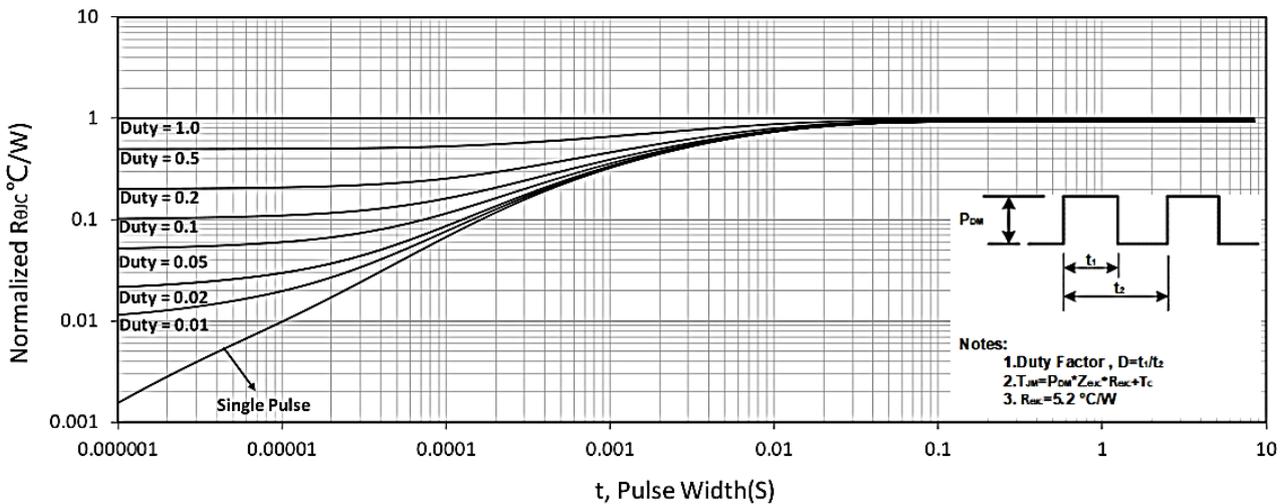
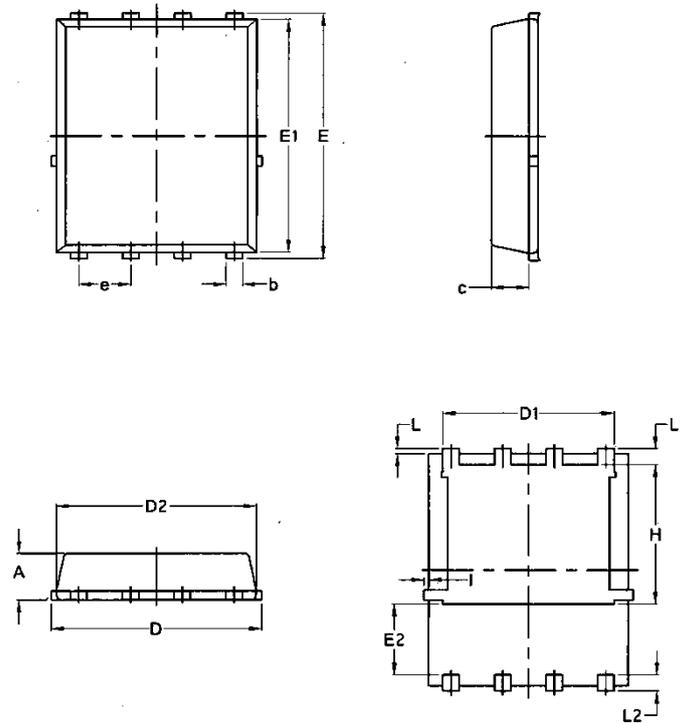


Figure 9 Normalized Maximum Transient Thermal Impedance

### Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

**30V N-Channel Enhancement Mode MOSFET****Attention**

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Edition	Date	Change
REV1.0	2023/3/31	Initial release

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