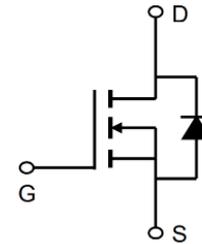


## 30V N-Channel Enhancement Mode MOSFET

### Description

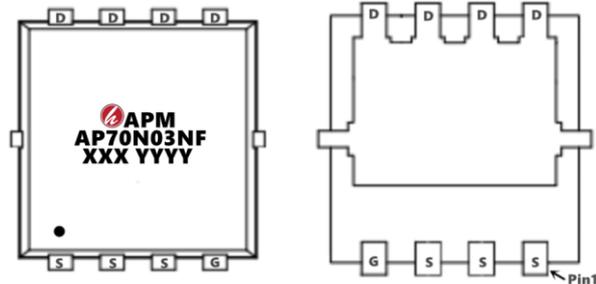
The AP70N03NF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

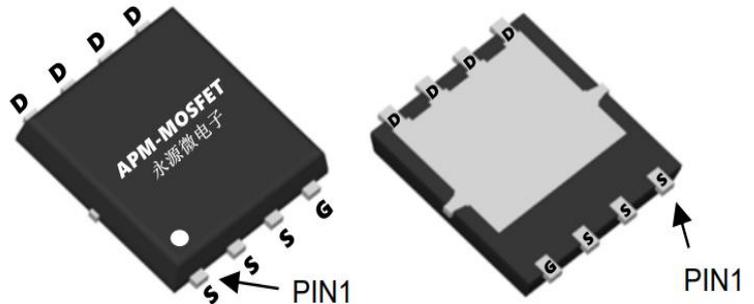
$V_{DS} = 30V$   $I_D = 70A$

$R_{DS(ON)} < 4.5m\Omega$  @  $V_{GS} = 10V$  (Type: 3.5m $\Omega$ )



### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP70N03NF	PDFN5*6-8L	AP70N03NF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	70	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	51	A
IDM	Pulsed Drain Current <sup>2</sup>	210	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	325	mJ
IAS	Avalanche Current	48	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation <sup>4</sup>	59	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation <sup>4</sup>	2	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	25	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.1	$^\circ C/W$

## 30V N-Channel Enhancement Mode MOSFET

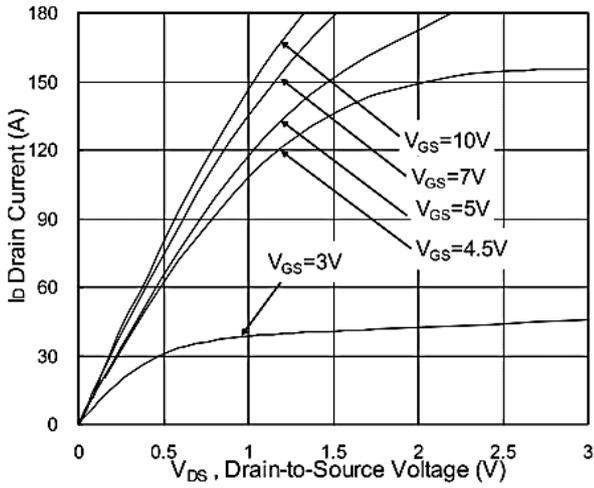
### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	33	---	V
RDS(ON)	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	---	3.5	4.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	---	6.5	8.5	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	1.6	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-6.16	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =30A	---	22	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.7	3.4	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A	---	20	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	7.6	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	7.2	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω I <sub>D</sub> =15A	---	7.8	---	ns
T <sub>r</sub>	Rise Time		---	15	---	
Td(off)	Turn-Off Delay Time		---	37.3	---	
T <sub>f</sub>	Fall Time		---	10.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	2295	---	pF
C <sub>oss</sub>	Output Capacitance		---	267	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	210	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	80	A
ISM	Pulsed Source Current <sup>2,5</sup>		---	---	160	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1	V
t <sub>rr</sub>	Reverse Recovery Time	IF=30A, dI/dt=100A/μs, T <sub>J</sub> =25°C	---	14	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	5	---	nC

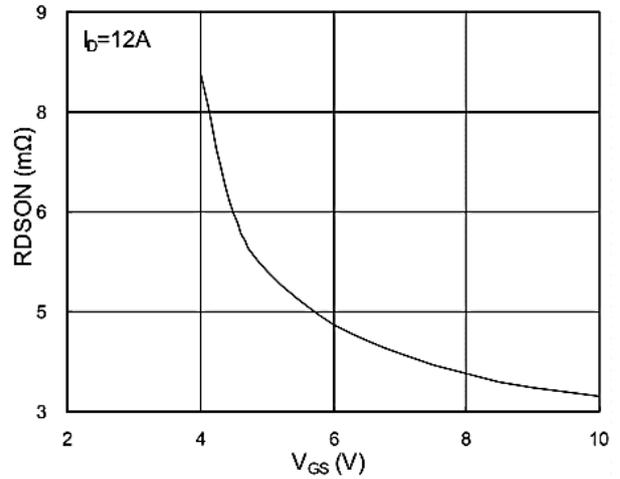
**Note :**

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=24V, V<sub>GS</sub>=10V, L=0.5mH, I<sub>AS</sub>=48A
- The power dissipation is limited by 175°C junction temperature
- The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

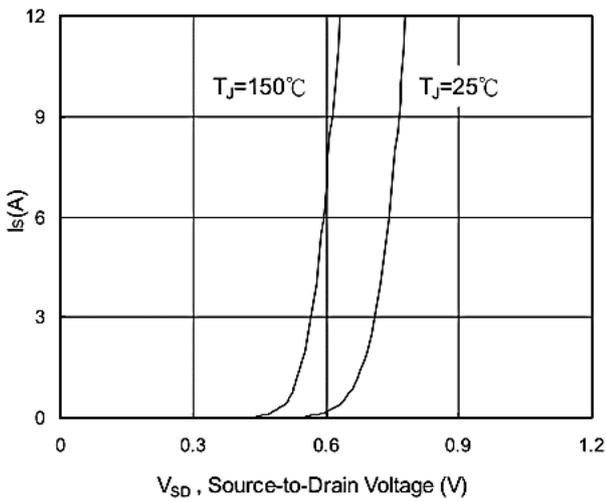
### Typical Characteristics



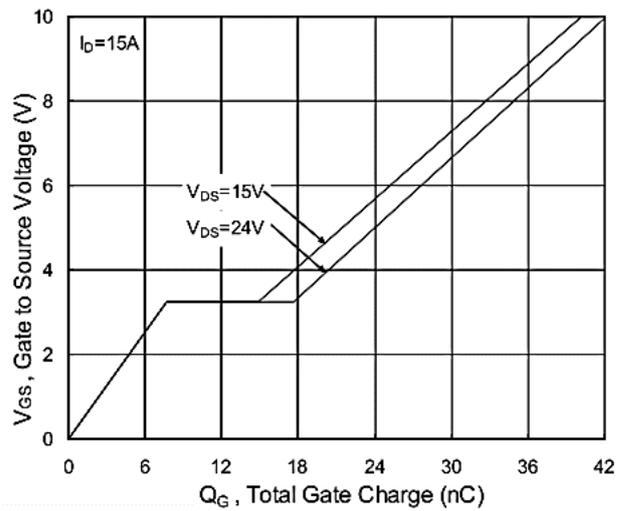
**Fig.1 Typical Output Characteristics**



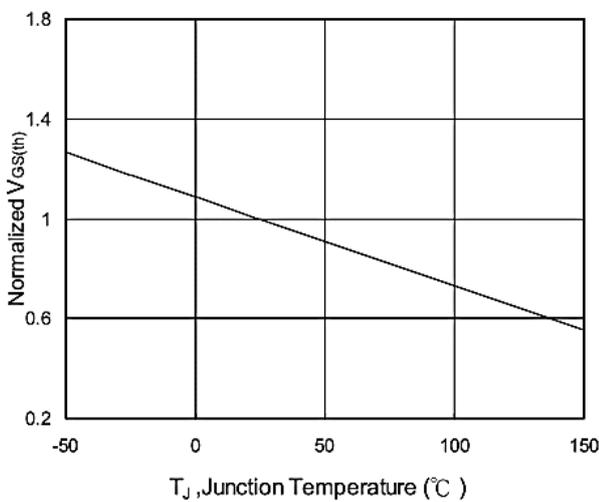
**Fig.2 On-Resistance vs. G-S Voltage**



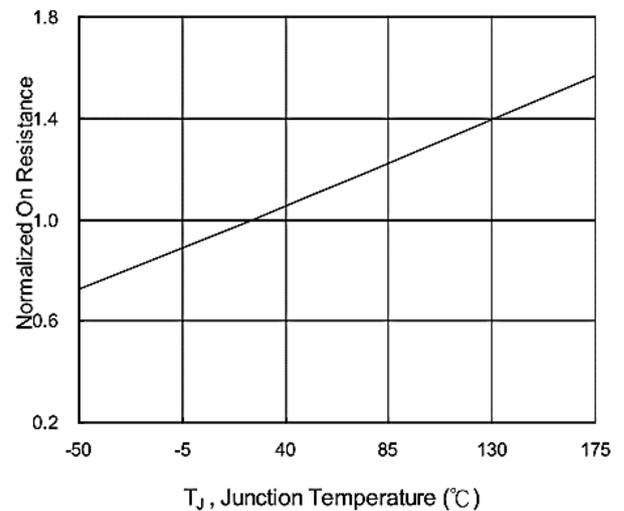
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



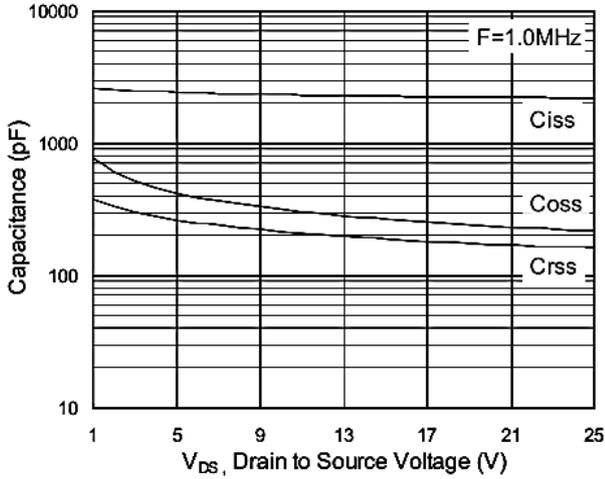
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



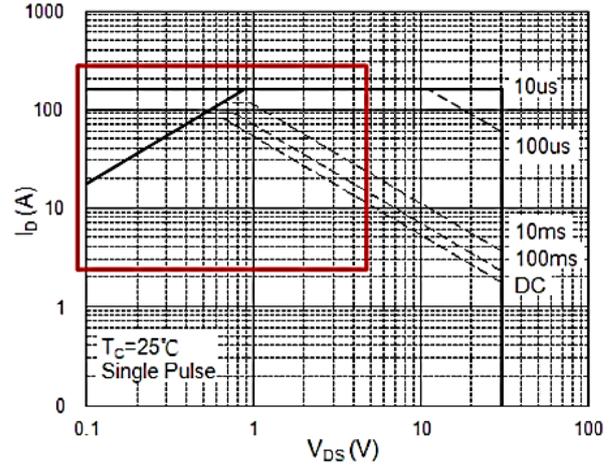
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



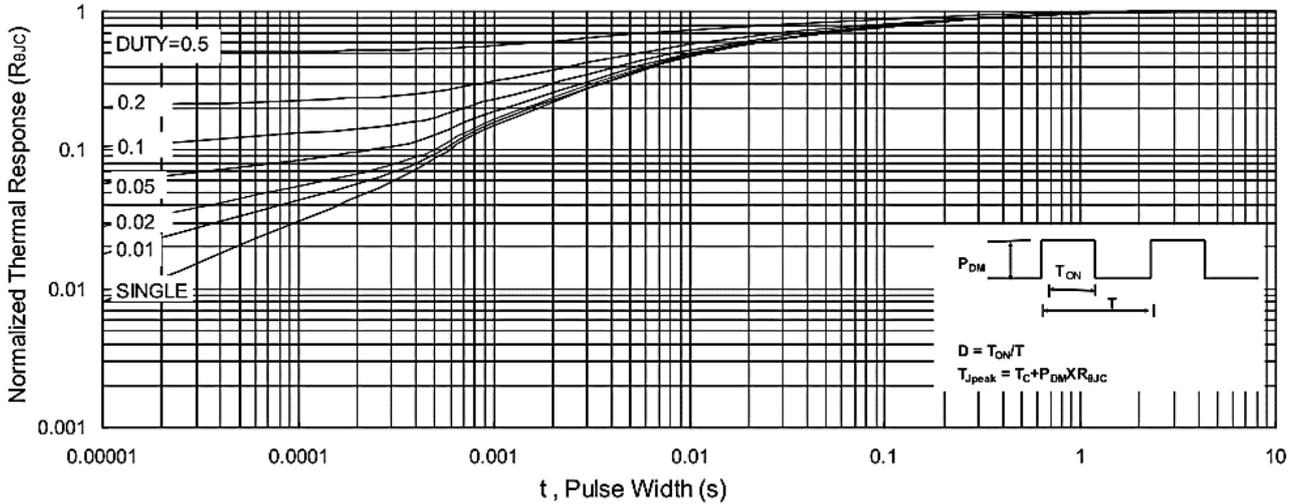
## 30V N-Channel Enhancement Mode MOSFET



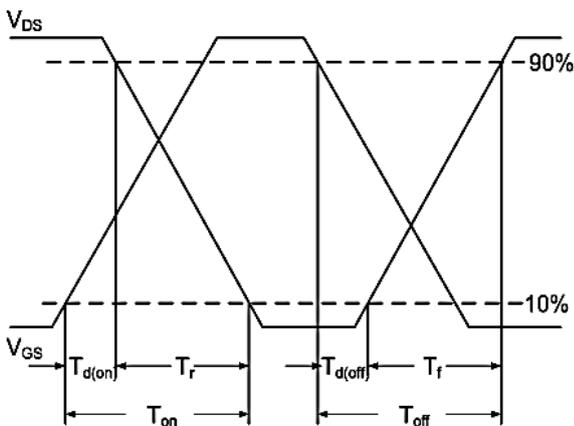
**Fig.7 Capacitance**



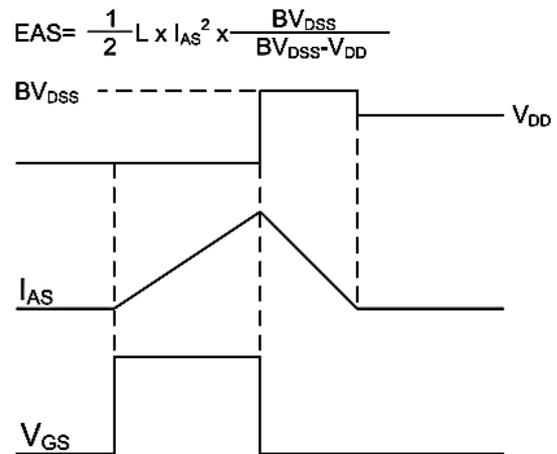
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

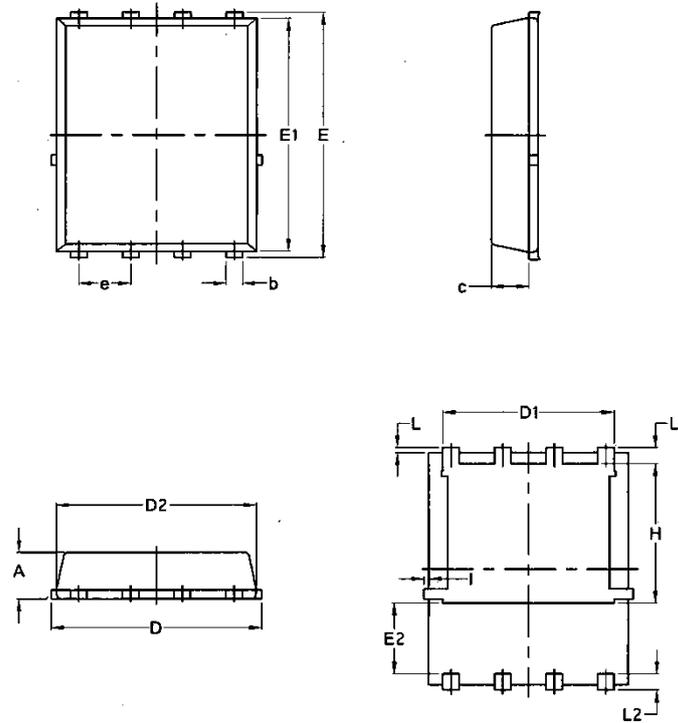


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

### Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

**30V N-Channel Enhancement Mode MOSFET****Attention**

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Rve1.1	2021/12/14	Reduce internal RDS

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