

## 30V N-Channel Enhancement Mode MOSFET

### Description

The AP70N03DF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

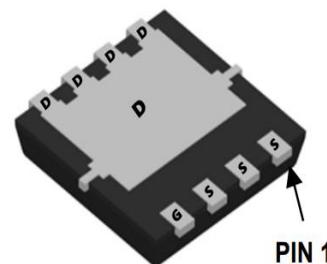
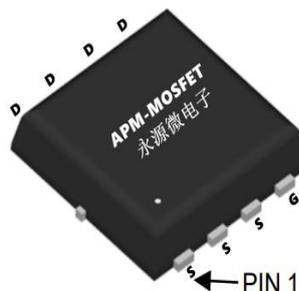
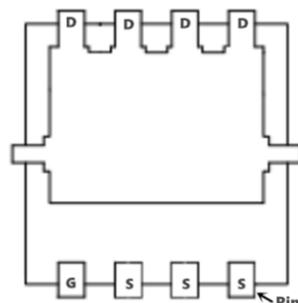
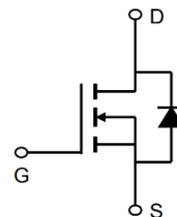
### General Features

$V_{DS} = 30V$   $I_D = 70A$

$R_{DS(ON)} < 4.5m\Omega$  @  $V_{GS}=10V$  (Type: 3.5m $\Omega$ )

### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP70N03DF	PDFN3*3-8L	AP70N03DF XXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	70	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	51	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	160	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	315	mJ
$I_{AS}$	Avalanche Current	38	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	59	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	2.1	$^\circ\text{C}/\text{W}$



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### Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	33	---	V
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=30A$	---	3.5	4.5	m $\Omega$
		$V_{GS}=4.5V, I_D=15A$	---	6.5	8.5	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-6.16	---	mV/ $^{\circ}\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^{\circ}\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	22	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.7	3.4	$\Omega$
Qg	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	20	---	nC
Qgs	Gate-Source Charge		---	7.6	---	
Qgd	Gate-Drain Charge		---	7.2	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	7.8	---	ns
Tr	Rise Time		---	15	---	
Td(off)	Turn-Off Delay Time		---	37.3	---	
Tf	Fall Time		---	10.6	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	2295	---	pF
Coss	Output Capacitance		---	267	---	
Crss	Reverse Transfer Capacitance		---	210	---	
Is	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	80	A
ISM	Pulsed Source Current <sup>2,5</sup>		---	---	160	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^{\circ}\text{C}$	---	---	1	V
trr	Reverse Recovery Time	$I_F=30A, di/dt=100A/\mu s, T_J=25^{\circ}\text{C}$	---	14	---	nS
Qrr	Reverse Recovery Charge		---	5	---	nC

**Note :**

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is  $V_{DD}=24V, V_{GS}=10V, L=0.5mH, I_{AS}=38A$
4. The power dissipation is limited by  $175^{\circ}\text{C}$  junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

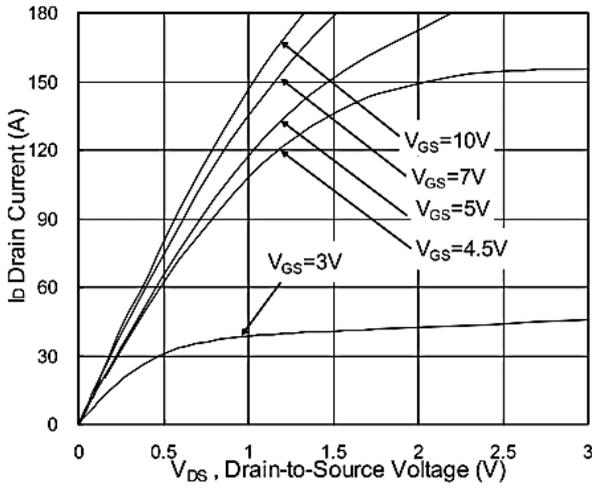


Fig.1 Typical Output Characteristics

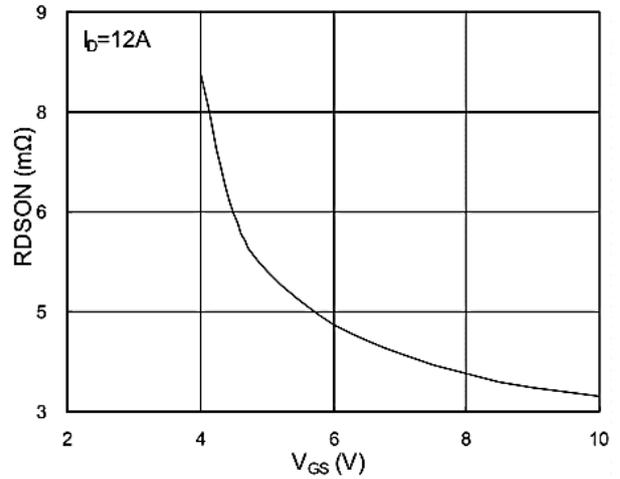


Fig.2 On-Resistance vs. G-S Voltage

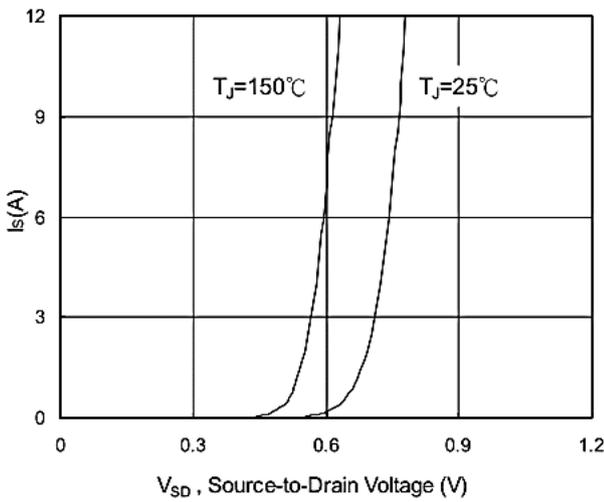


Fig.3 Forward Characteristics of Reverse

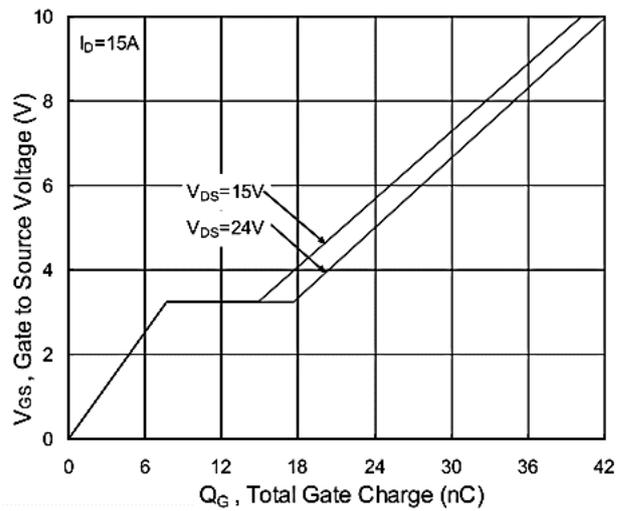


Fig.4 Gate-Charge Characteristics

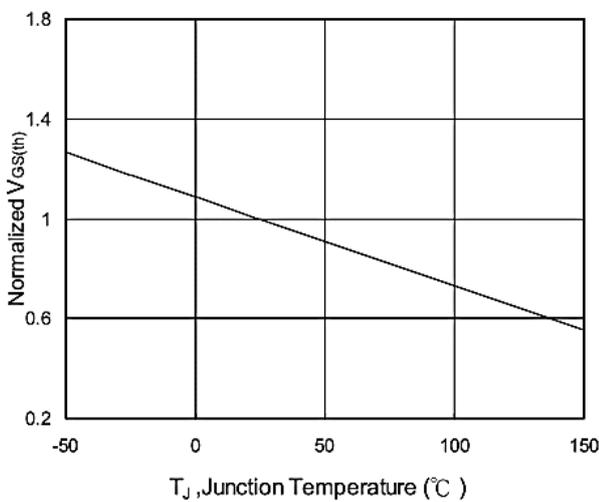


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

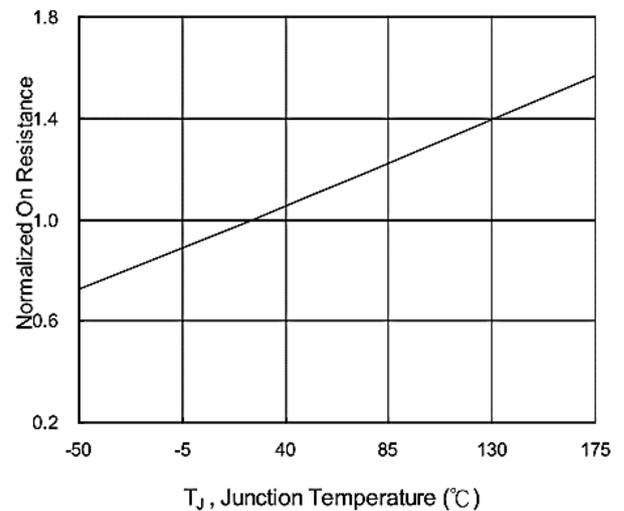
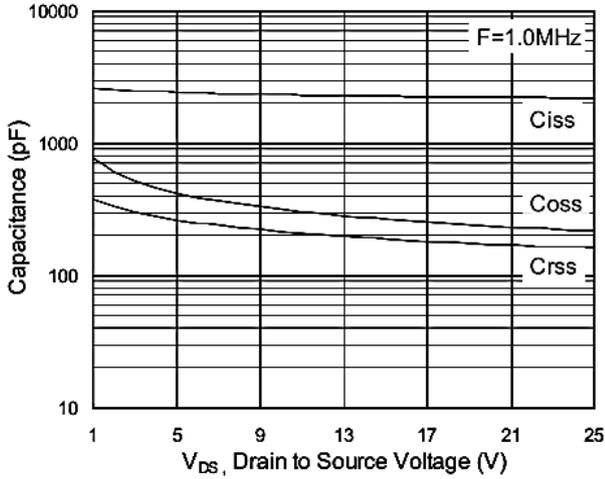


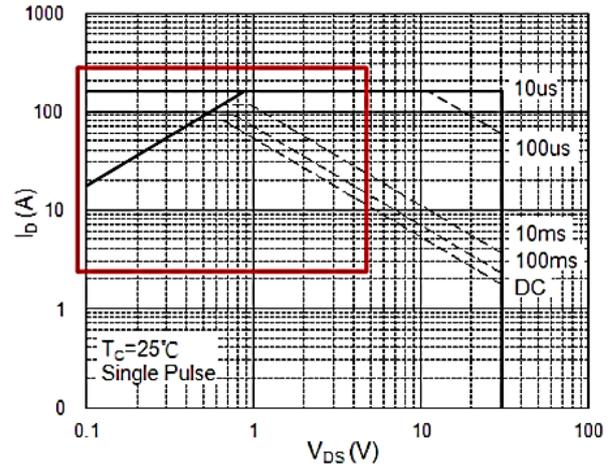
Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



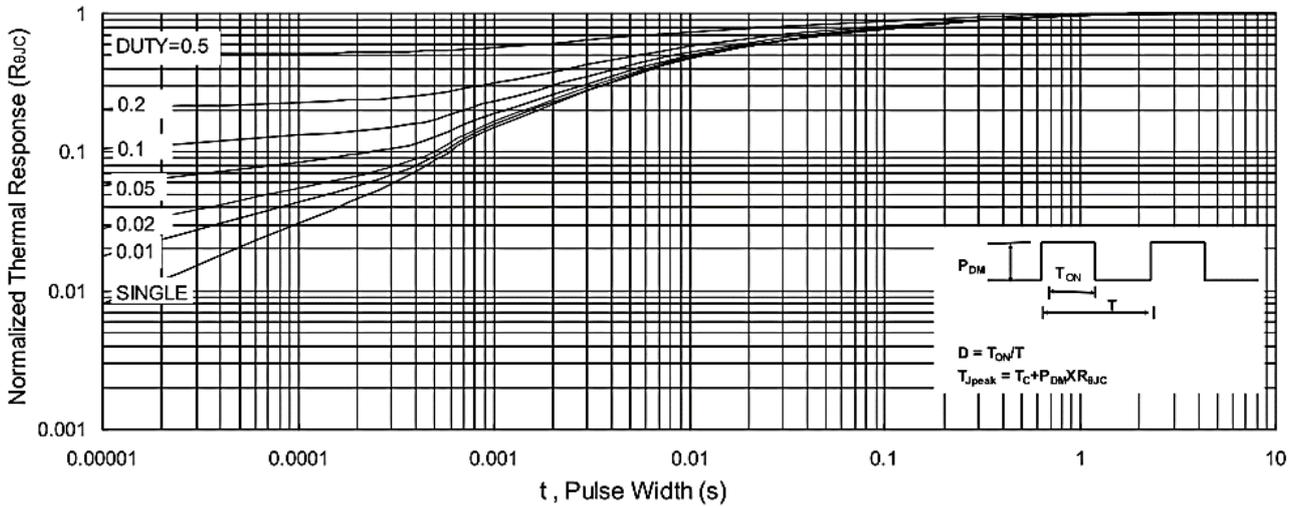
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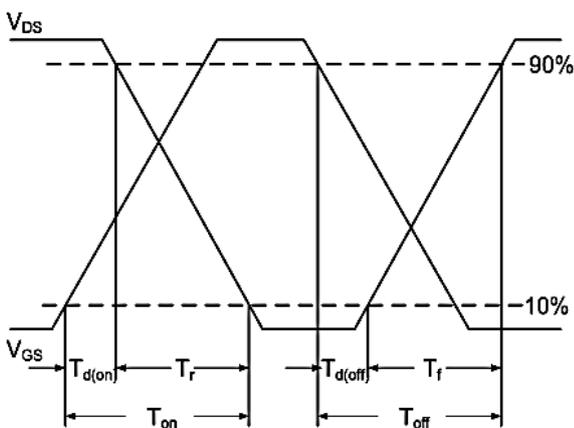
**Fig.7 Capacitance**



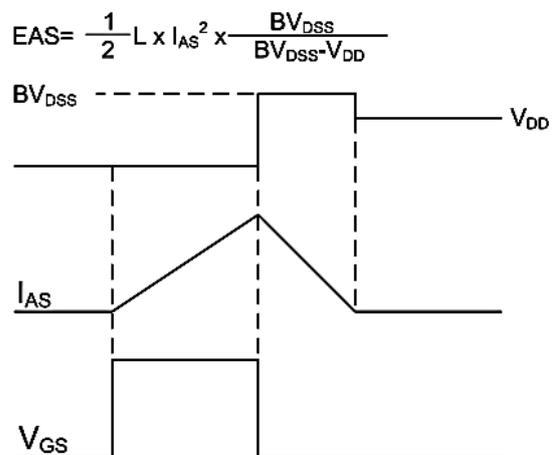
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

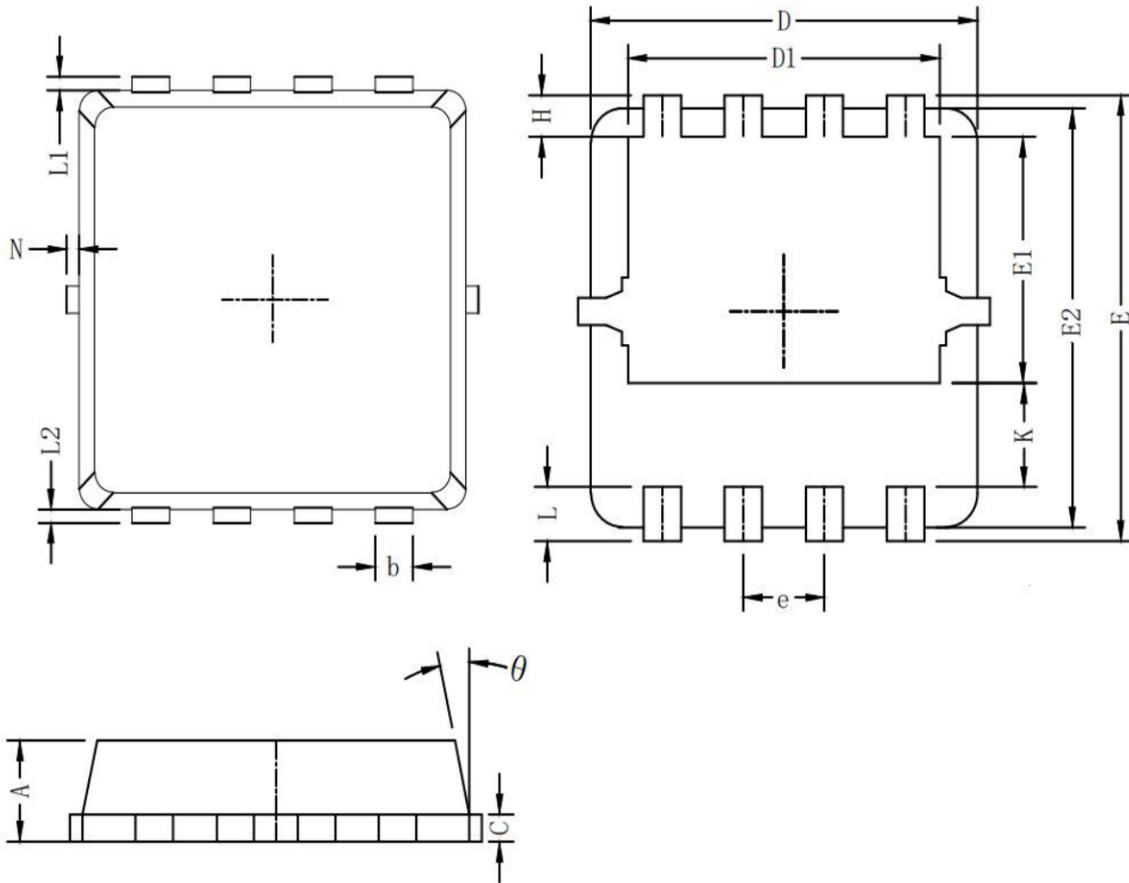


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

Package Mechanical Data-PDFN3\*3-8L- Single



Symbol	Dim in mm		
	min.	typ.	max.
A	0.6	0.75	0.9
b	0.2	0.3	0.4
C	0.15	0.2	0.25
D	3	3.1	3.2
D1	2.3	2.45	2.6
E	3.15	3.3	3.45
E1	1.43	1.73	1.93
E2	2.9	3.05	3.2
e	0.65BSC		
H	0.2	0.35	0.5
K	0.57	0.77	0.87
L	0.3	0.4	0.5
L1/L2	0.1REF		
$\theta$	8°	10°	13°
N	0		0.15

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<b>Edition</b>	<b>Date</b>	<b>Change</b>
Rve1.0	2019/8/1	Initial release
Rve1.1	2021/12/14	Reduce internal RDS
Rve1.2	2025/8/1	Update LOGO And Corrected Manual POD

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