AP65N03DF

30V N-Channel Enhancement Mode MOSFET

Description

The AP65N03DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS}=30V I_D =65A

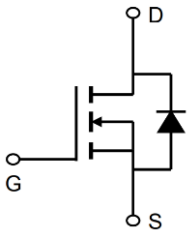
$R_{DS(ON)}$ < 5.5mΩ @ V_{GS}=10V **(Type：4.0mΩ)**

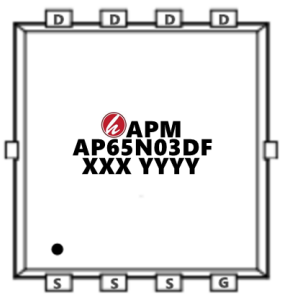
Application

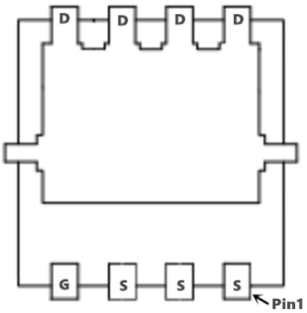
Battery protection

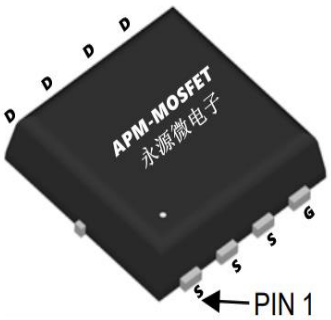
Load switch

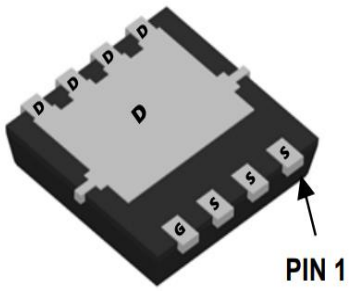
Uninterruptible power supply











Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP65N03DF	PDFN3*3-8L	AP65N03DF XXXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	65	A
I_D@T_C=75℃	Continuous Drain Current, V_{GS} @ 10V[1]	45	A
I_{DM}	Pulsed Drain Current[2]	240	A
EAS	Single Pulse Avalanche Energy[3]	256	mJ
I_{AS}	Avalanche Current	15	A
P_D@T_C=25℃	Total Power Dissipation[4]	46	W
P_D@T_A=25℃	Total Power Dissipation[4]	2.72	W
T_{STG}	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	2.72	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	30	33	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} =30V, V_{GS} = 0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS} =0V,V_{GS} = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1.0	1.6	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS} =10V, I_D =30A	-	4.0	5.5	mΩ
		V_{GS} =4.5V, I_D =20A	-	6.1	8.5	
Ciss	Input Capacitance	V_{DS} =15V, V_{GS} =0V, f = 1.0MHz	-	1614	-	pF
Coss	Output Capacitance		-	245	-	pF
Crss	Reverse Transfer Capacitance		-	215	-	pF
Q_g	Total Gate Charge	V_{DS} =15V, I_D =30A, V_{GS} =10V	-	33.7	-	nC
Qgs	Gate-Source Charge		-	8.5	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	7.5	-	nC
td(on)	Turn-on Delay Time	V_{DS}=15V, I_D=30A, R_{GEN}=3Ω, V_{GS} =10V	-	7.5	-	ns
t_r	Turn-on Rise Time		-	14.5	-	ns
td(off)	Turn-off Delay Time		-	35.2	-	ns
t_f	Turn-off Fall Time		-	9.6	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	70	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	280	A
VSD	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S=30A	-	-	1.2	V

Note :

1、The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is VDD=24V,VGS=10V,L=0.5mH,IAS=18A

4、The power dissipation is limited by 175℃ junction temperature

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

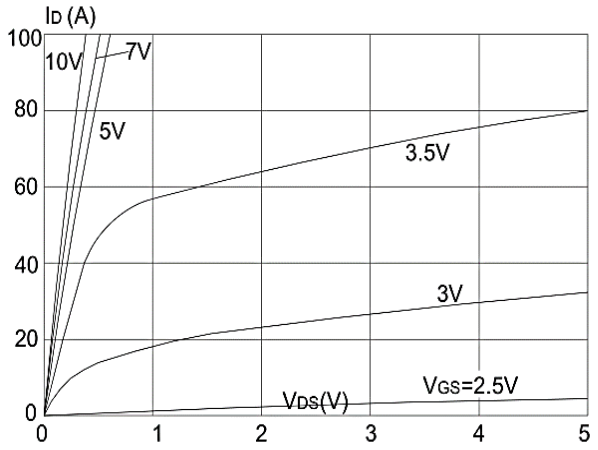


Figure1: Output Characteristics

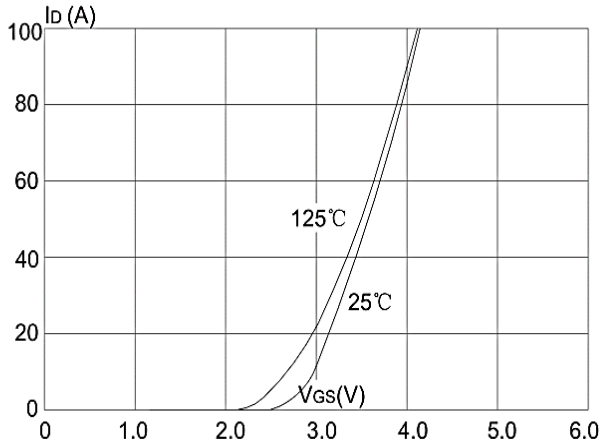


Figure 2: Typical Transfer Characteristics

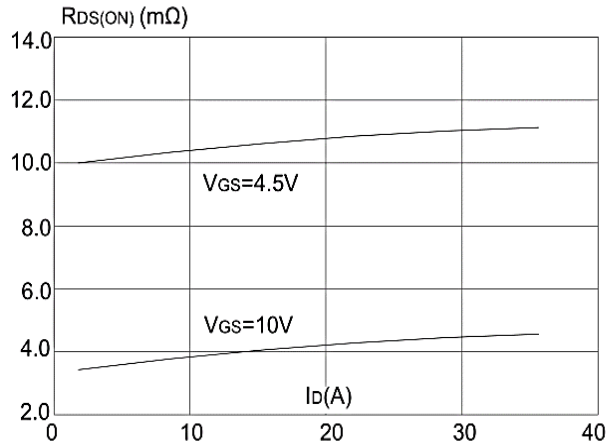


Figure 3:On-resistance vs. Drain Current

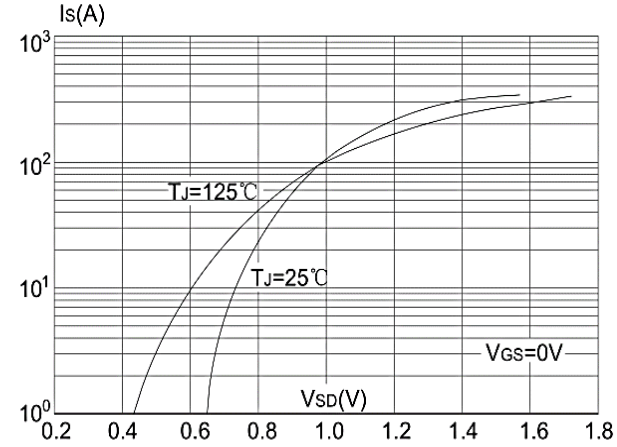


Figure 4: Body Diode Characteristics

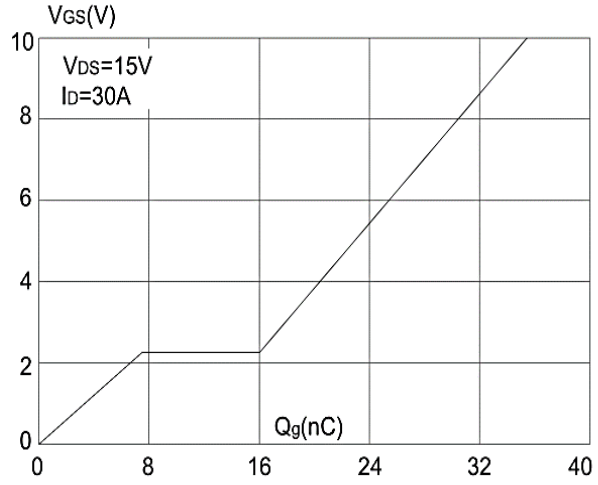


Figure 5: Gate Charge Characteristics

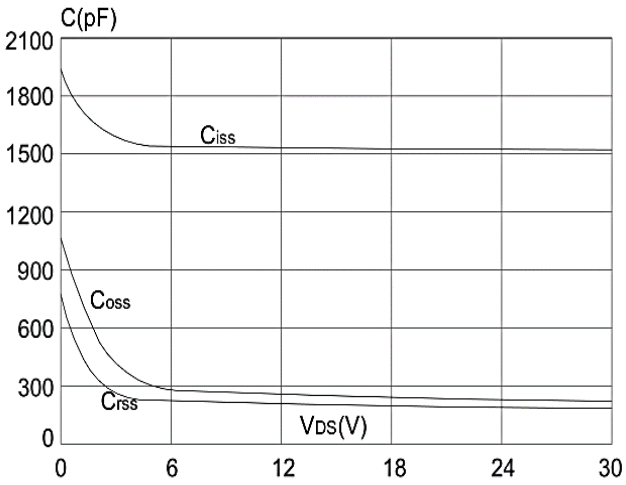


Figure 6: Capacitance Characteristics

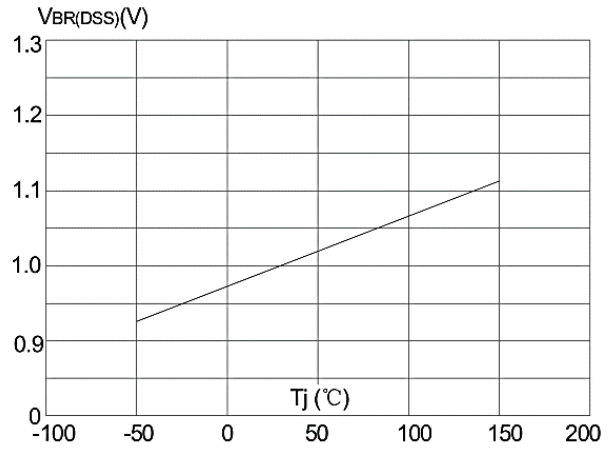


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

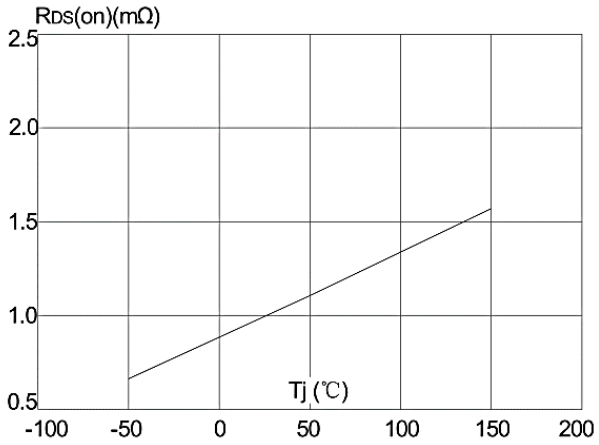


Figure 8: Normalized on Resistance vs Junction Temperature

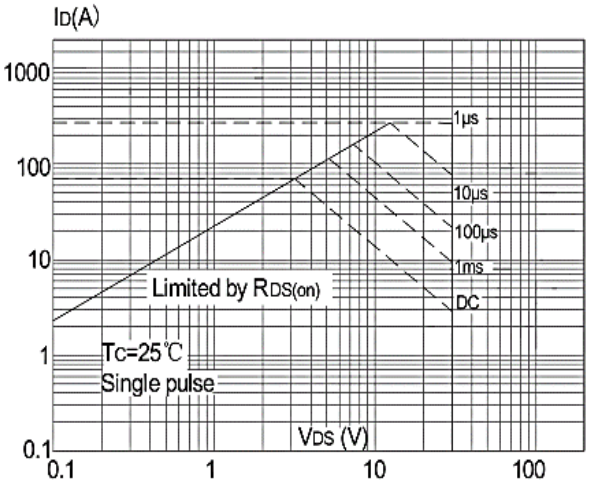


Figure 9: Maximum Safe Operating Area vs. Case Temperature

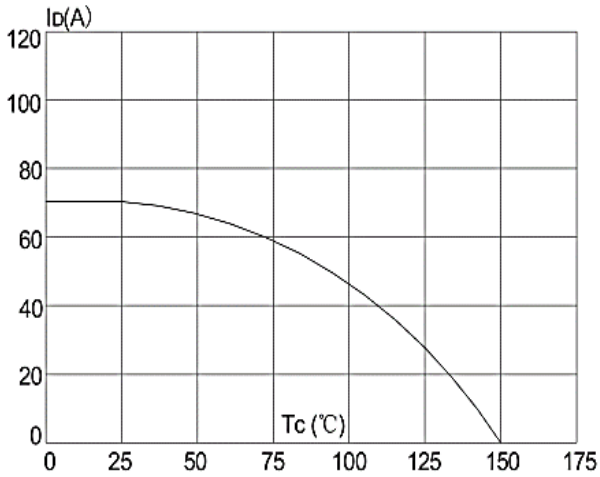


Figure 10: Maximum Continuous Drain Current

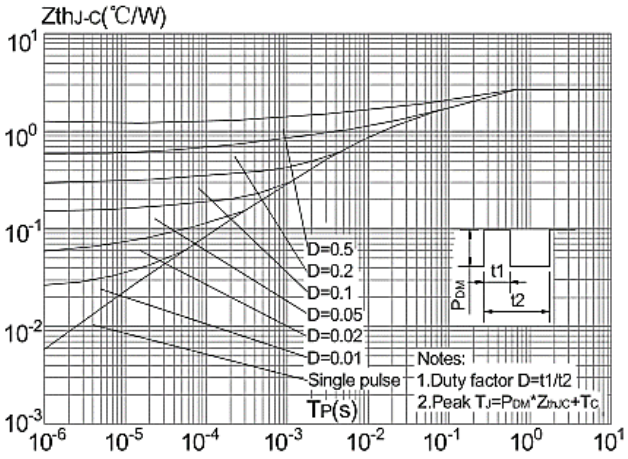
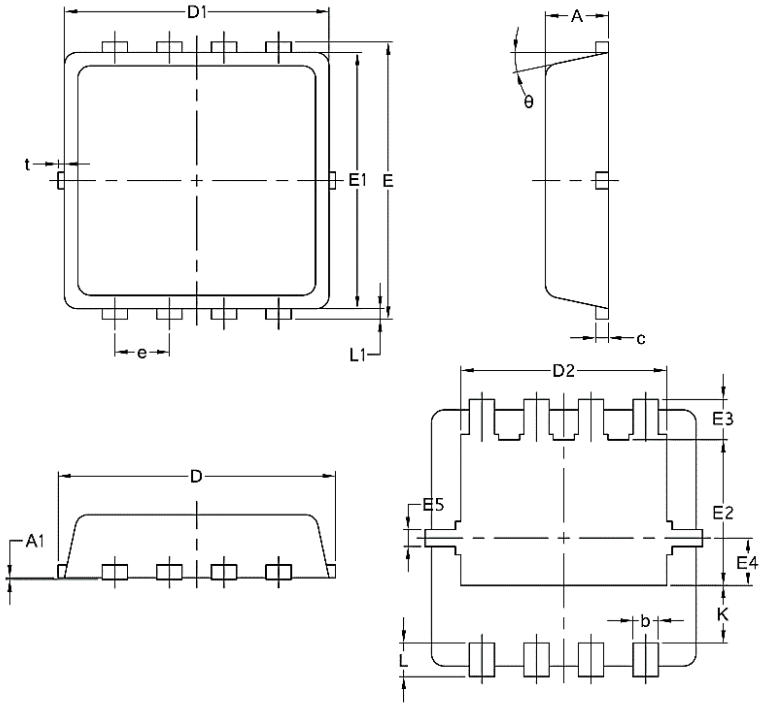


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ca

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

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30V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/5/1	Initial release
Rve1.1	2021/12/14	Reduce RDS