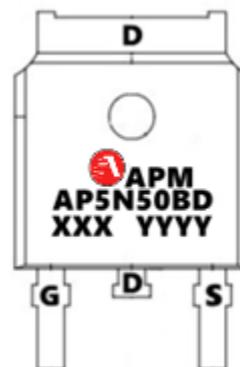
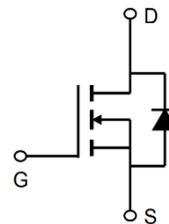


500V N-Channel Enhancement Mode MOSFET

Description

The AP5N50BD is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

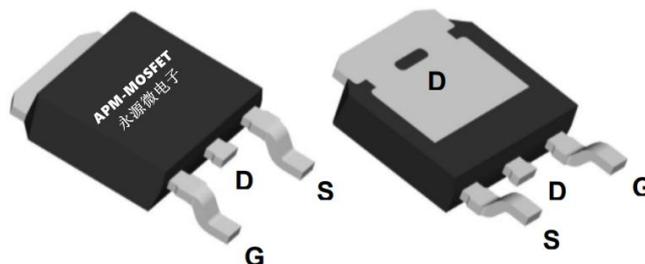
$V_{DS} = 500V$ $I_D = 5A$

$R_{DS(ON)} < 3.0\Omega$ @ $V_{GS}=10V$ (Type: 2.4 Ω)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N50BD	TO252-3L	AP5N50BD XXX YYYY	2500

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	500	V
I_D	Continuous Drain Current	5	A
I_{DM}	Pulsed Drain Current (note1)	15	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	57	mJ
I_{AR}	Avalanche Current (note1)	2.4	A
E_{AR}	Repetitive Avalanche Energy (note1)	6.4	mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	32.9	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55~+150	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	6.25	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ C/W$



500V N-Channel Enhancement Mode MOSFET

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	500	550	--	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
IGSS	Gate-Source Leakage	$V_{GS} = \pm 30V$	--	--	± 100	nA
VGS(th)	Gate-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.0	3.0	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	$V_{GS} = 10V, I_D = 3.5A$	--	2.4	3.0	Ω
Ciss	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$	--	310	--	pF
Coss	Output Capacitance		--	39	--	
Crss	Reverse Transfer Capacitance		--	6	--	
Qg	Total Gate Charge	$V_{DD} = 400V, I_D = 3A, V_{GS} = 10V$	--	8	--	nC
Qgs	Gate-Source Charge		--	1.2	--	
Qgd	Gate-Drain Charge		--	5	--	
td(on)	Turn-on Delay Time	$V_{DD} = 250V, I_D = 3A, R_G = 25\Omega$	--	7.8	--	ns
tr	Turn-on Rise Time		--	33	--	
td(off)	Turn-off Delay Time		--	23	--	
tr	Turn-off Fall Time		--	59	--	
IS	Continuous Body Diode Current	$T_C = 25^\circ\text{C}$	--	--	3.0	A
ISM	Pulsed Diode Forward Current		--	--	12	A
VSD	Body Diode Voltage	$T_J = 25^\circ\text{C}, I_{SD} = 3A, V_{GS} = 0V$	--	--	1.4	V
trr	Reverse Recovery Time	$V_{GS} = 0V, I_S = 3A, di_F/dt = 100A/\mu s$	--	80	--	ns
Qrr	Reverse Recovery Charge		--	1.8	--	μC

Note :

- 1、 The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . IAS = 2.4A, VDD = 50V, RG = 25 Ω , Starting TJ = 25 $^\circ\text{C}$
- 3、 The test condition is Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 1\%$
- 4、 The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

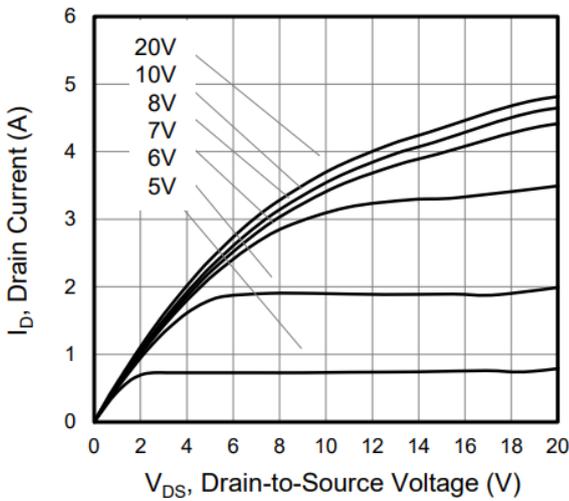


Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

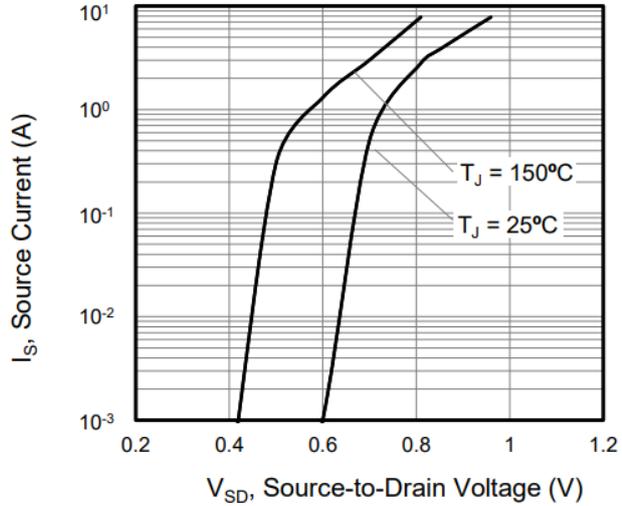


Figure 2. Body Diode Forward Voltage

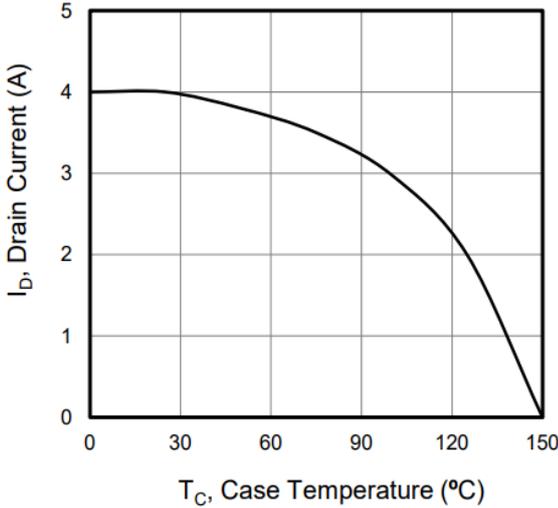


Figure 3. Drain Current vs. Temperature

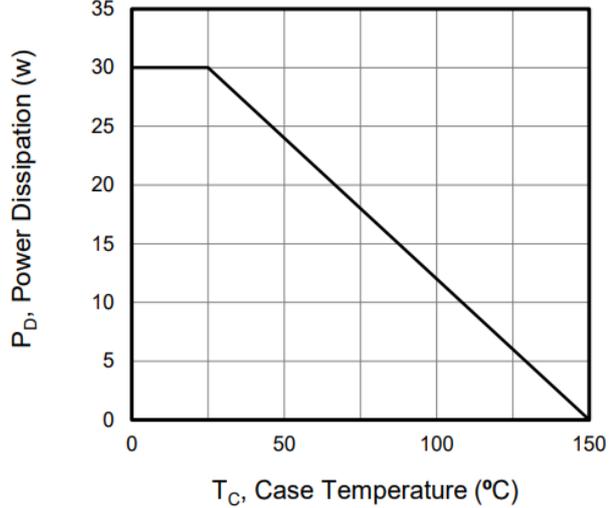


Figure 4. BV DSS Variation vs. Temperature

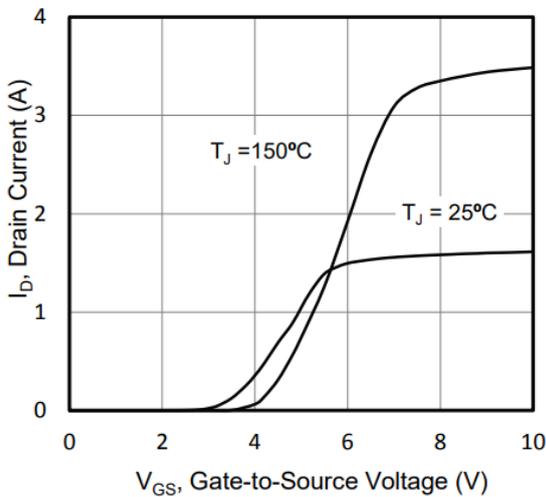


Figure 5. Transfer Characteristics

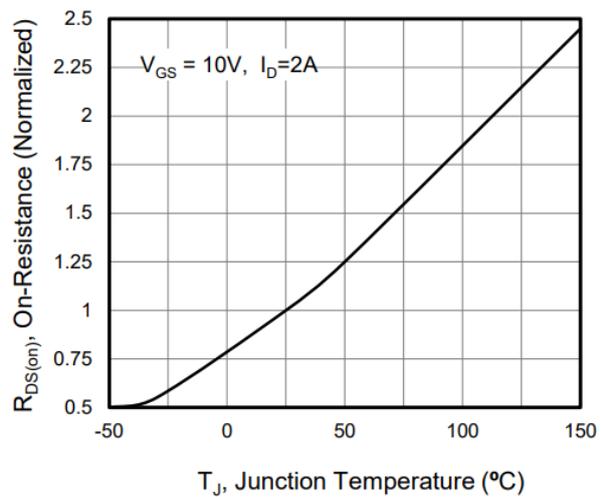


Figure 6. On-Resistance vs. Temperature

500V N-Channel Enhancement Mode MOSFET

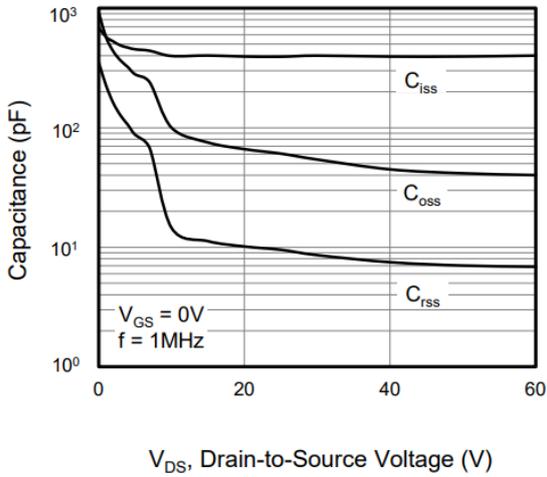


Figure 7. Capacitance

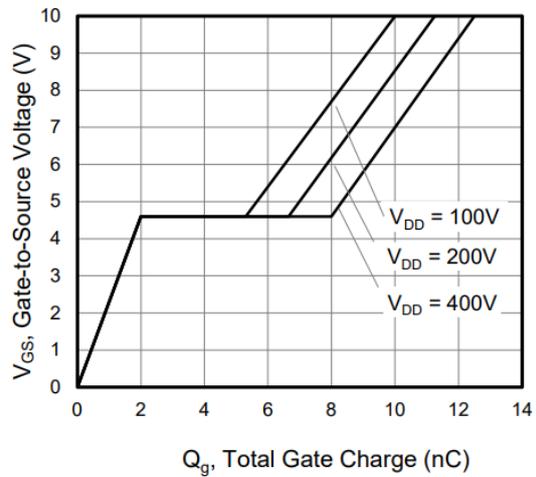


Figure 8. Gate Charge

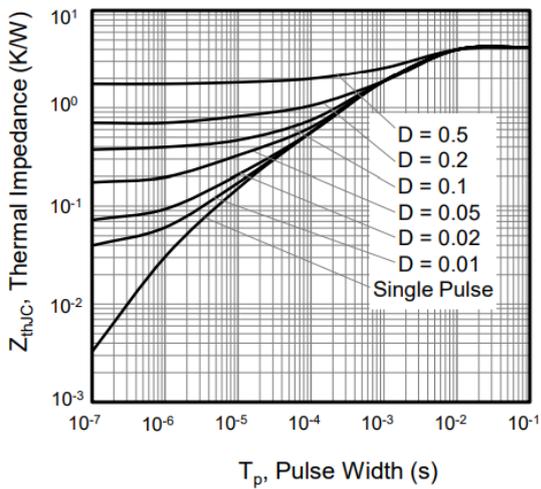
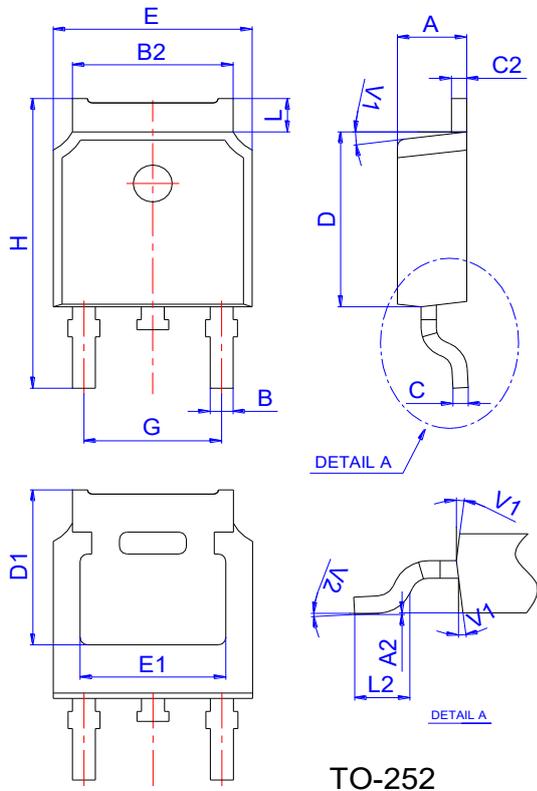


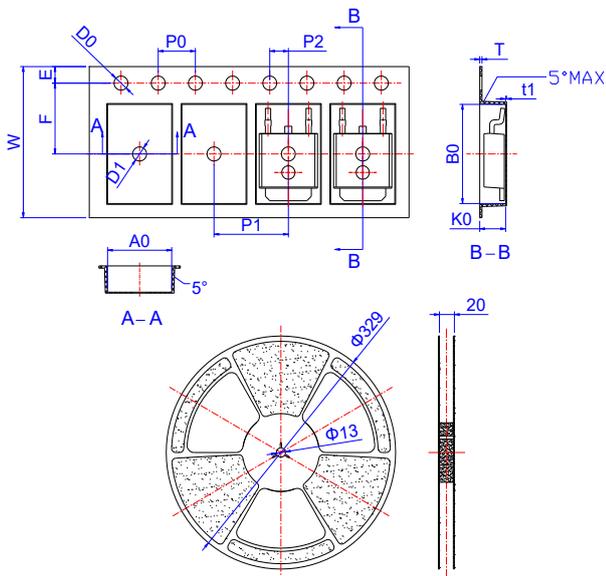
Figure 9. Transient Thermal Impedance

Package Mechanical Data



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

500V N-Channel Enhancement Mode MOSFET

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Edition	Date	Change
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Rve1.1	2025/11/06	Update LOGO

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