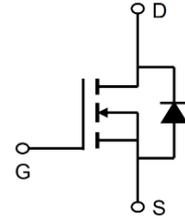


## 100V N-Channel Enhancement Mode MOSFET

### Description

The AP5N10SI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = 100V$   $I_D = 5A$

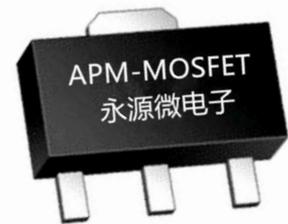
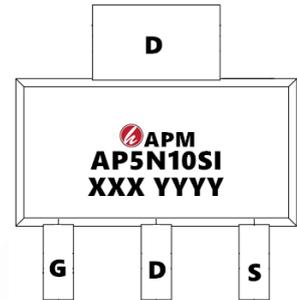
$R_{DS(ON)} < 110m\Omega$  @  $V_{GS}=10V$

### Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N10SI	SOT89-3L	AP5N10SI XXX YYYY	3000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.6	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	15	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>3</sup>	3.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	40	$^\circ C/W$



## 100V N-Channel Enhancement Mode MOSFET

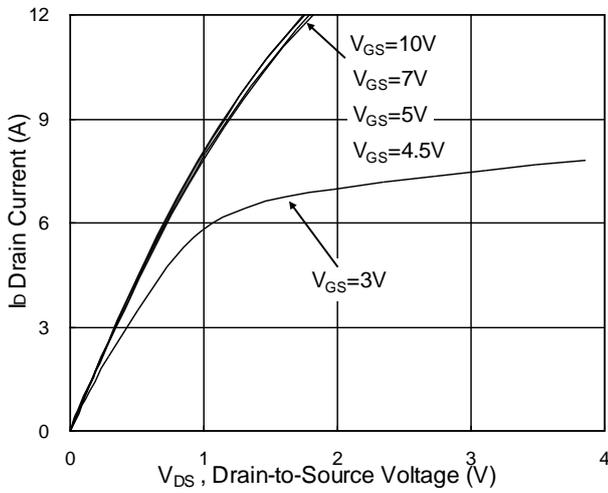
### Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	---	---	V
ΔBVDSS/ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.122	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =3A	---	88	110	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	---	95	125	mΩ
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.6	2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	-4.84	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	10	uA
		V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	100	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =2A	---	10.2	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	2.3	4.6	Ω
Q <sub>g</sub>	Total Gate Charge (10V)	V <sub>DS</sub> =60V, V <sub>GS</sub> =10V, I <sub>D</sub> =2A	---	25.5	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	4.2	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	4.3	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =50V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =1A	---	17.3	---	ns
T <sub>r</sub>	Rise Time		---	2.8	---	
Td(off)	Turn-Off Delay Time		---	50	---	
T <sub>f</sub>	Fall Time		---	2.8	---	
Ciss	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	677	---	pF
Coss	Output Capacitance		---	46	---	
Crss	Reverse Transfer Capacitance		---	32	---	
IS	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	2	A
ISM	Pulsed Source Current <sup>2,4</sup>		---	---	4	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

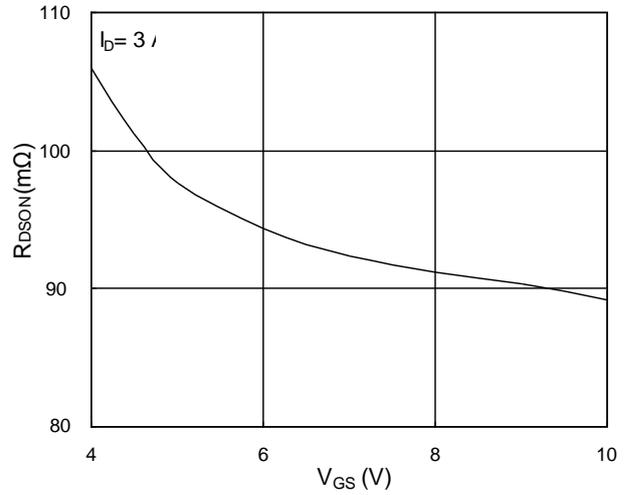
#### Note :

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

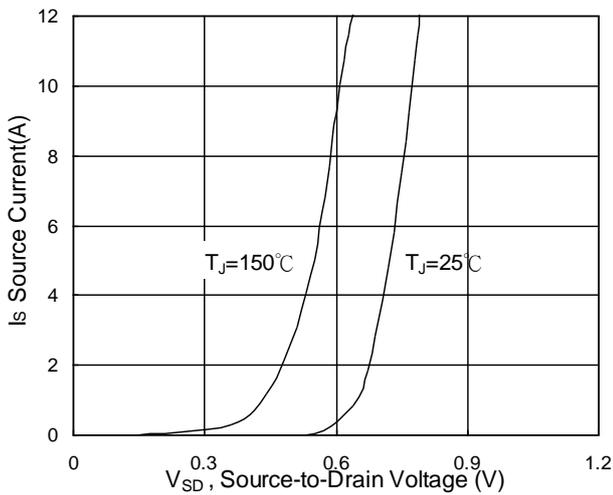
**Typical Characteristics**



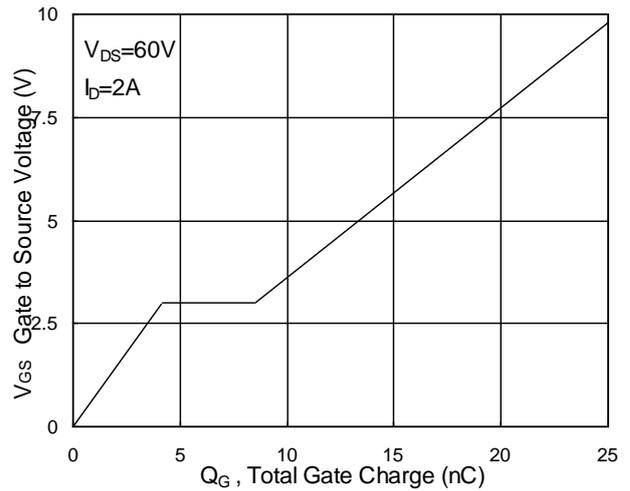
**Fig.1 Typical Output Characteristics**



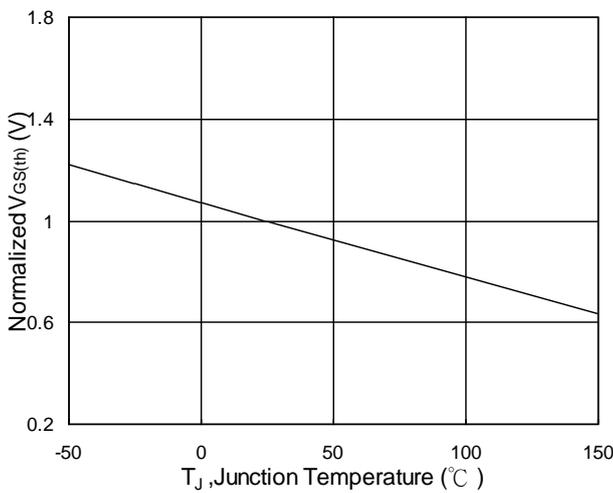
**Fig.2 On-Resistance vs. Gate-Source**



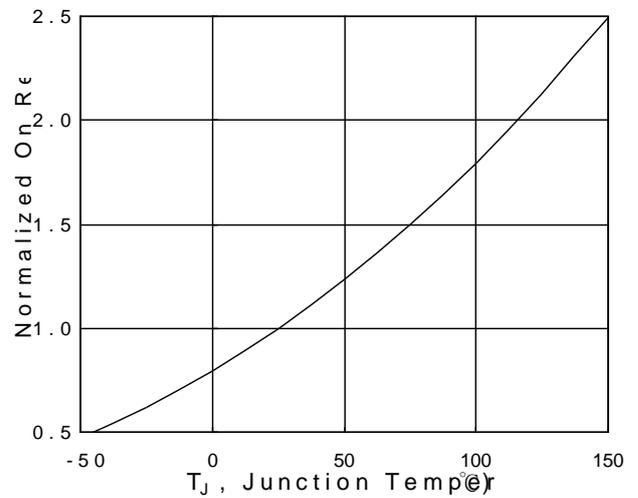
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**



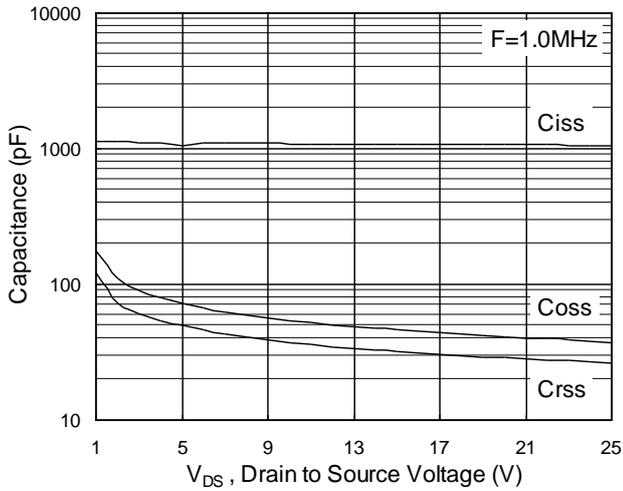
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



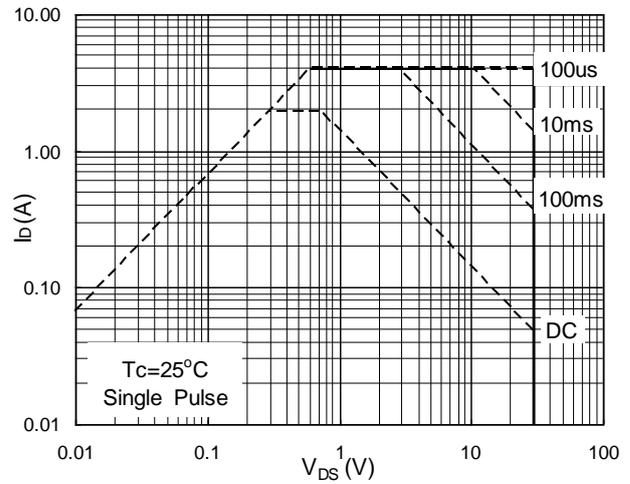
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



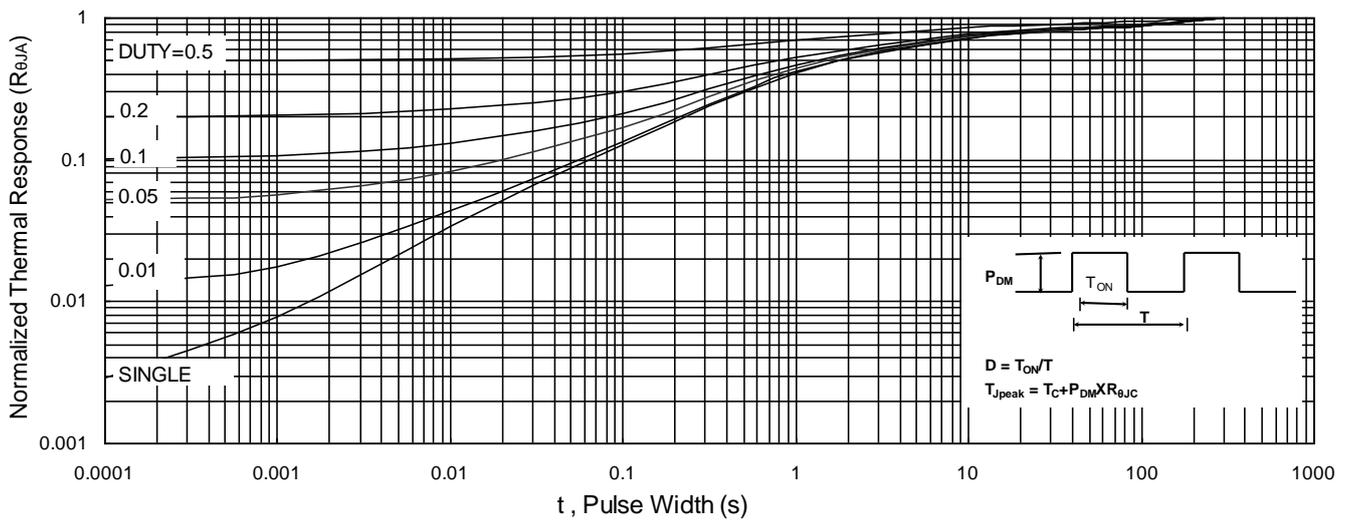
**100V N-Channel Enhancement Mode MOSFET**



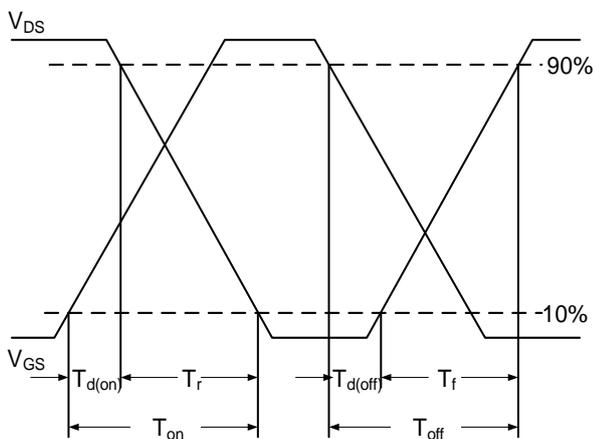
**Fig.7 Capacitance**



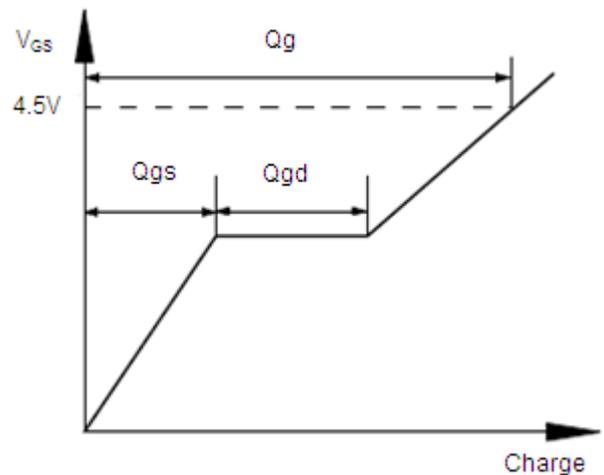
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

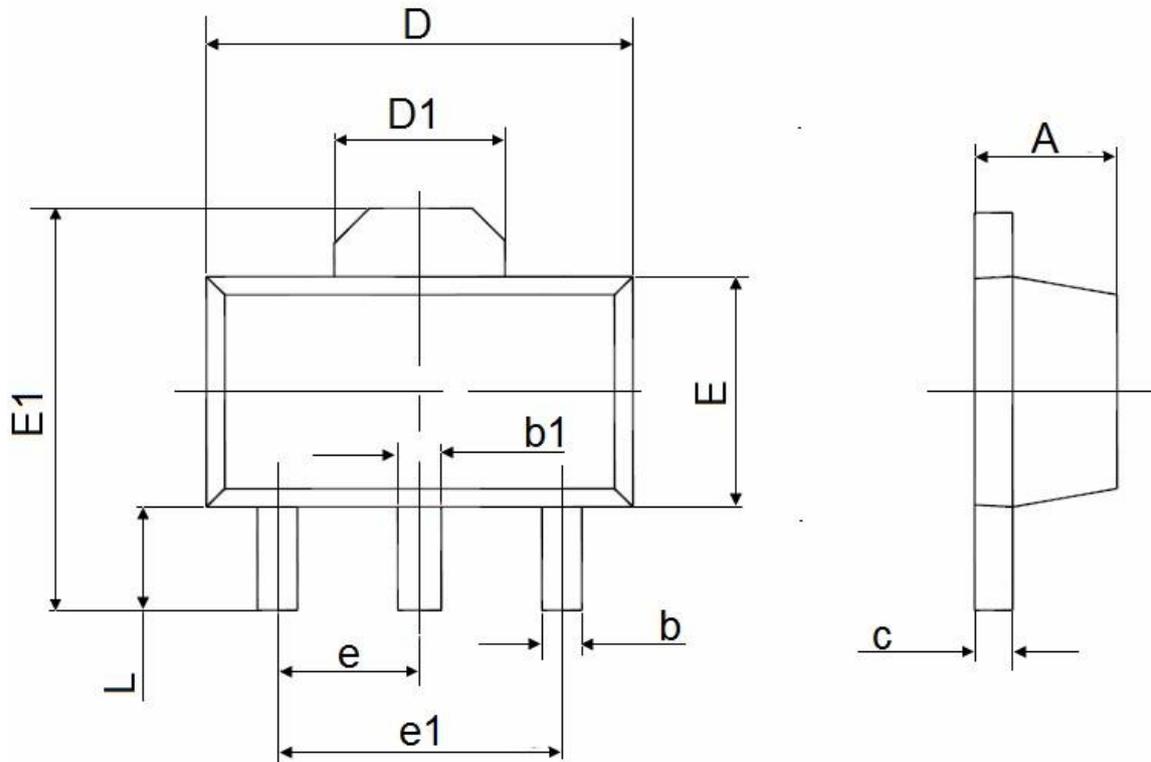


**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**

Package Mechanical Data-SOT89-3L-YX



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047

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**100V N-Channel Enhancement Mode MOSFET**

<b>Edition</b>	<b>Date</b>	<b>Change</b>
Rve3.8	2017/6/10	Initial release
Rve3.9	2019/12/01	Reduce RDS(on) and Ciss

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