

## 40V N-Channel Enhancement Mode MOSFET

### Description

The AP5N04MI uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 40V$   $I_D = 5A$

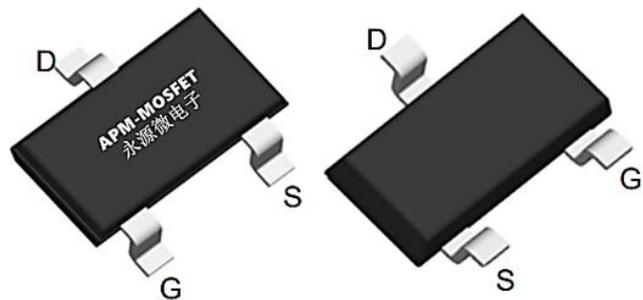
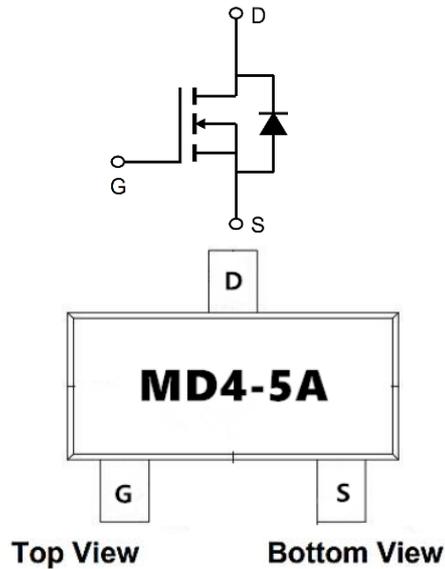
$R_{DS(ON)} < 37m\Omega$  @  $V_{GS}=10V$  (Type: 28m $\Omega$ )

### Application

Wireless charging

Boost driver

LED



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5N04MI	SOT23-3L	MD4-5A	3000

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.5	A
IDM	Pulsed Drain Current <sup>2</sup>	14	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	16.2	mJ
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	1	W
TSTG	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	125	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	80	$^\circ C/W$

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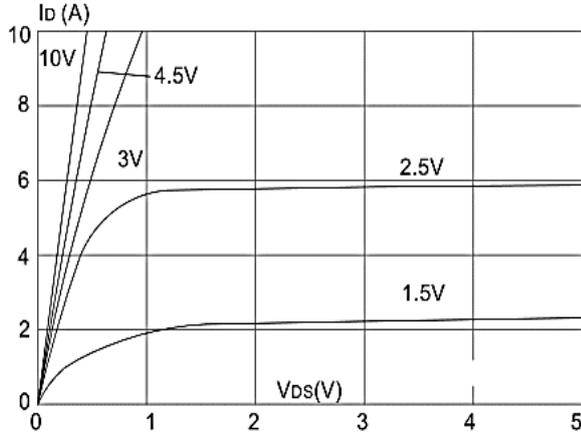
### Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	44	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.032	---	V/ $^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=4A$	---	28	37	m $\Omega$
		$V_{GS}=4.5V, I_D=3A$	---	40	50	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.5	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=4A$	---	8	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.4	4.8	$\Omega$
Qg	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=3A$	---	5	---	nC
Qgs	Gate-Source Charge		---	1.54	---	
Qgd	Gate-Drain Charge		---	1.84	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V,$ $R_G=3.3\Omega$ $I_D=1A$	---	7.8	---	ns
Tr	Rise Time		---	2.1	---	
Td(off)	Turn-Off Delay Time		---	29	---	
Tf	Fall Time		---	2.1	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	452	---	pF
Coss	Output Capacitance		---	51	---	
Crss	Reverse Transfer Capacitance		---	38	---	
IS	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	4.5	A
ISM	Pulsed Source Current <sup>2,4</sup>		---	---	14	A
VSD	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

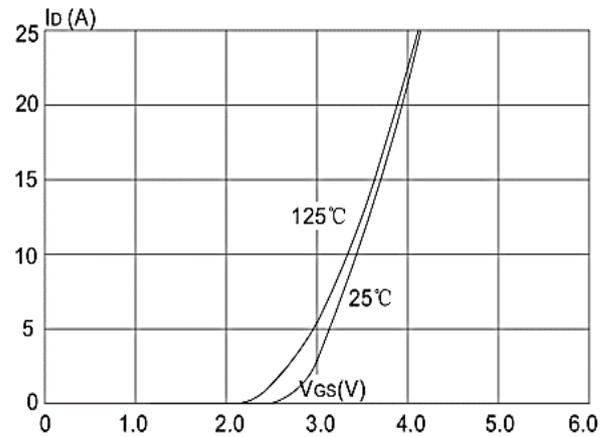
**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4、The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

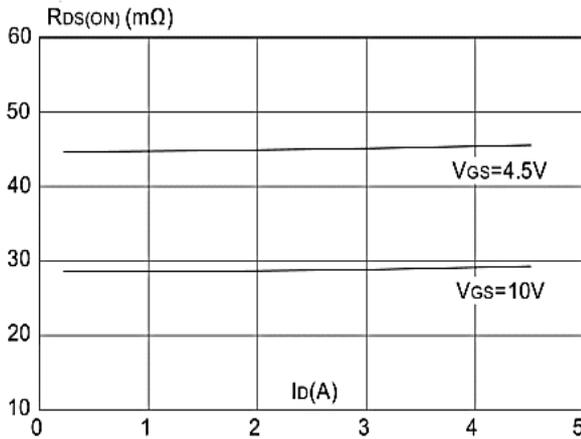
**N-Typical Characteristics**



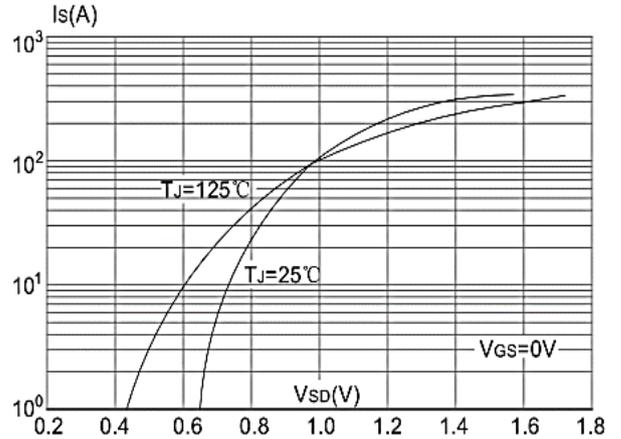
**Figure 1: Output Characteristics**



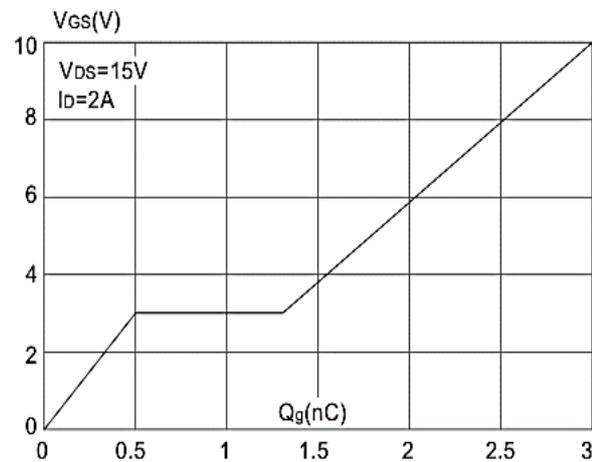
**Figure 2: Typical Transfer Characteristics**



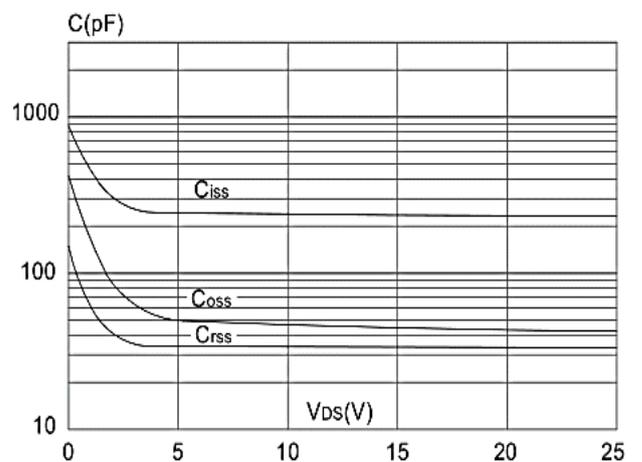
**Figure 3: On-resistance vs. Drain Current**



**Figure 4: Body Diode Characteristics**

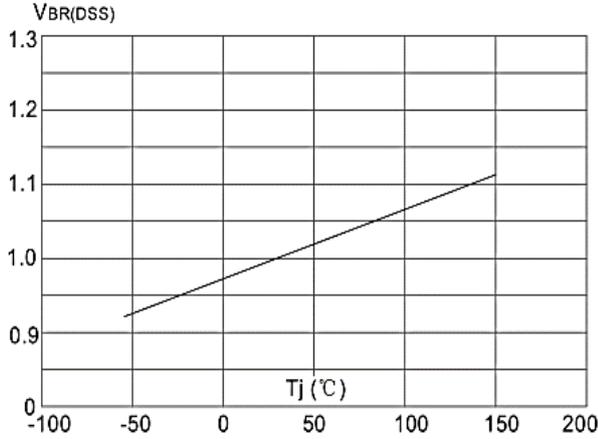


**Figure 5: Gate Charge Characteristics**

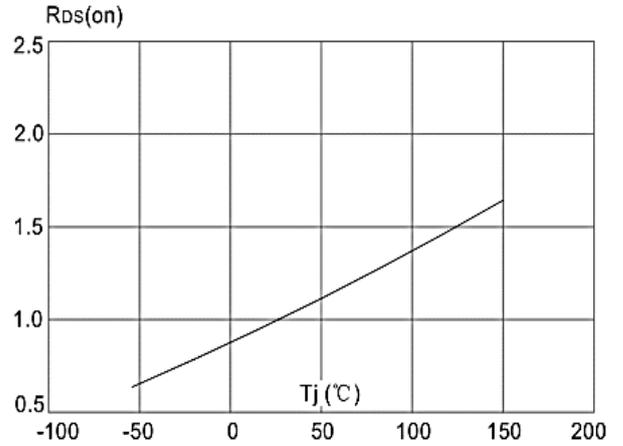


**Figure 6: Capacitance Characteristics**

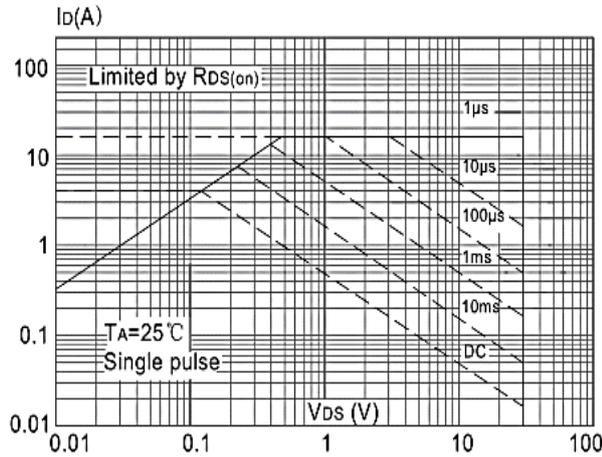
**40V N-Channel Enhancement Mode MOSFET**



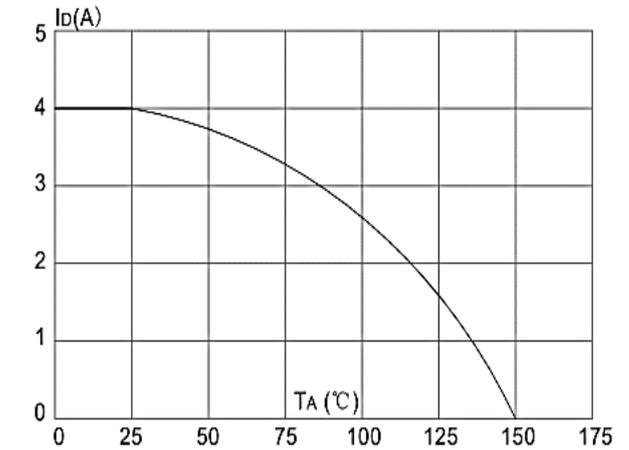
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



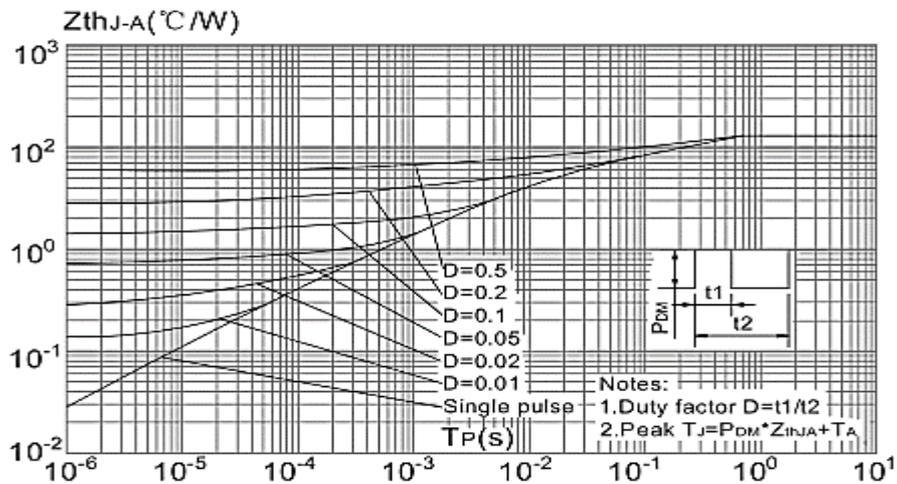
**Figure 8: Normalized on Resistance vs. Junction Temperature**



**Figure 9: Maximum Safe Operating Area vs. Case Temperature**

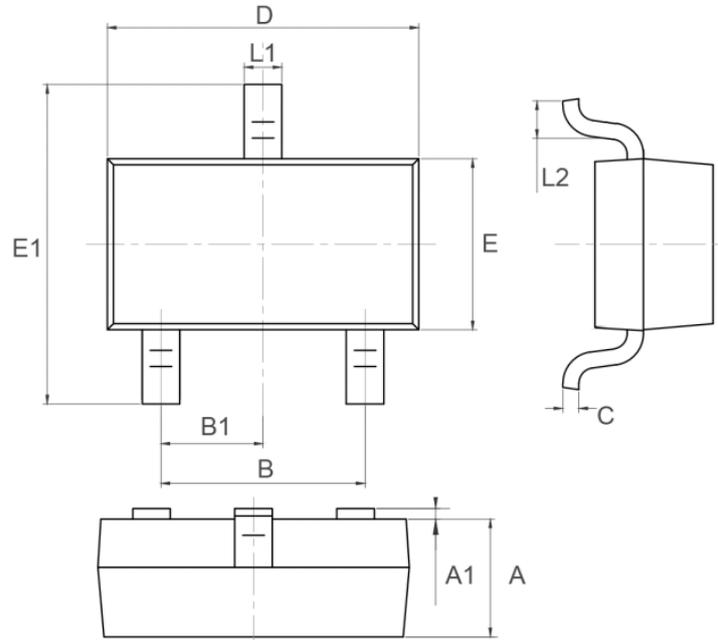


**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case**

Package Mechanical Data-SOT23-3L-Single



Symbol	Dimensions in Millimeters		
	MIN.	TYP.	MAX.
A	1	1.1	1.2
A1	0	0.05	0.1
B	1.8	1.9	2
B1	0.95TYP		
C	0.1	0.15	0.2
D	2.82	2.92	3.02
E	1.5	1.6	1.7
E1	2.65	2.8	2.95
L1	0.3	0.4	0.5
L2	0.3	0.45	0.6

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Edition	Date	Change
REV3.8	2018/1/31	Initial release
REV3.9	2023/8/19	Change layout

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