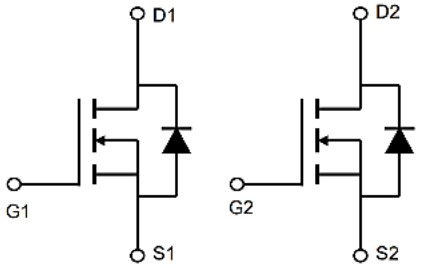
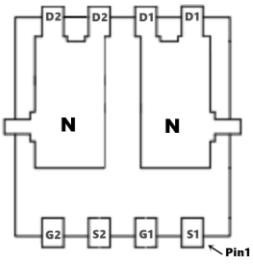
AP50H06NF

60V N+N-Channel Enhancement Mode MOSFET

Description

The AP50H06NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.





General Features

V_{DS} = 60V I_D =50A

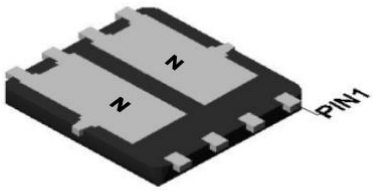
$R_{DS(ON)}$ < 16mΩ @ V_{GS}=10V (Type：11mΩ)

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50H06NF	PDFN5*6-8L	AP50H06NF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	60	V
VGS	Gate-Source Voltage	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	50	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	25	A
IDM	Pulsed Drain Current[2]	150	A
EAS	Single Pulse Avalanche Energy[3]	64	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	3.6	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta}JC$	Thermal Resistance Junction-Case[1]	2.8	℃/W
$R_{\theta}JA$	Thermal Resistance Junction-Ambient [1]	25	℃/W

60V N+N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	60	65	---	V
△BVDSS/△TJ	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.057	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=12A	---	11	16	mΩ
		V_{GS}=4.5V , I_D=10A	---	15	20	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.2	1.6	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.68	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=48V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=48V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=15A	---	45	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=48V , V_{GS}=4.5V , I_D=15A	---	19.3	---	nC
Q_{gs}	Gate-Source Charge		---	7.1	---	
Q_{gd}	Gate-Drain Charge		---	7.6	---	
Td(on)	Turn-On Delay Time	V_{DD}=30V , V_{GS}=10V , R_G=3.3Ω, I_D=15A	---	7.2	---	ns
T_r	Rise Time		---	50	---	
Td(off)	Turn-Off Delay Time		---	36.4	---	
T_f	Fall Time		---	7.6	---	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	2423	---	pF
Coss	Output Capacitance		---	145	---	
Crss	Reverse Transfer Capacitance		---	97	---	
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	35	A
ISM	Pulsed Source Current[2,5]		---	---	80	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=A , T_J=25℃	---	---	1	V
t_{rr}	Reverse Recovery Time	IF=15A , dI/dt=100A/μs , T_J=25℃	---	16.3	---	nS
Q_{rr}	Reverse Recovery Charge		---	11	---	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The EAS data shows Max. rating . The test condition is VDD=48V,VGS=10V, L=0.1mH IAS=25A, starting Tj=25 °C

5、The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

Typical Characteristics

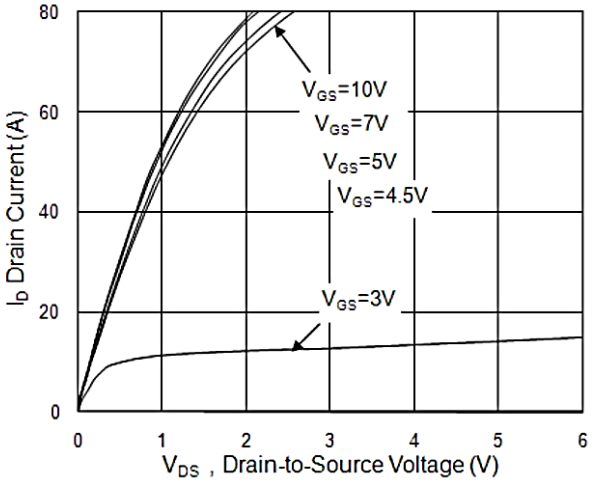


Fig.1 Typical Output Characteristics

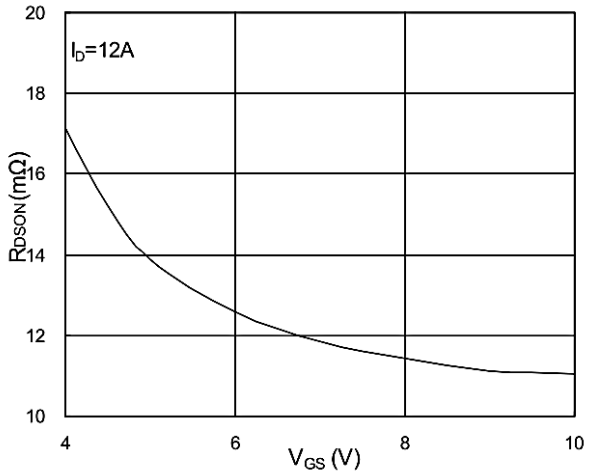


Fig.2 On-Resistance v.s Gate-Source

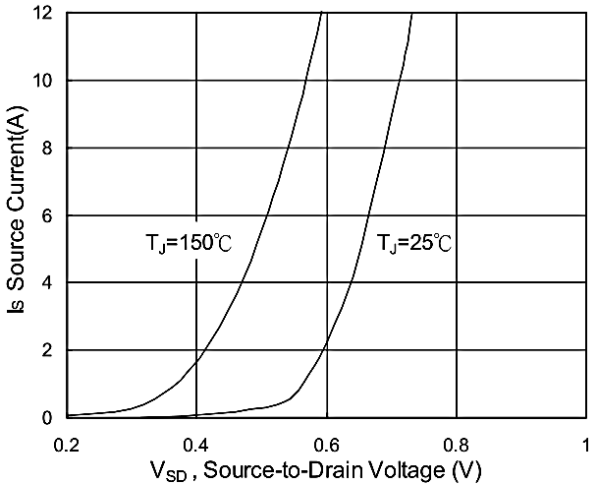


Fig.3 Forward Characteristics of Reverse

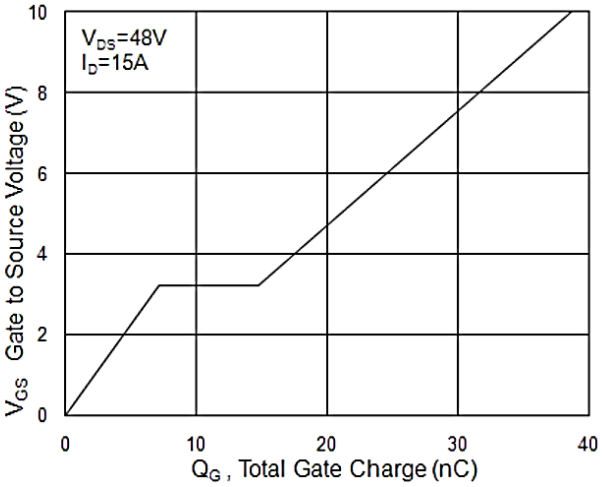


Fig.4 Gate-Charge Characteristics

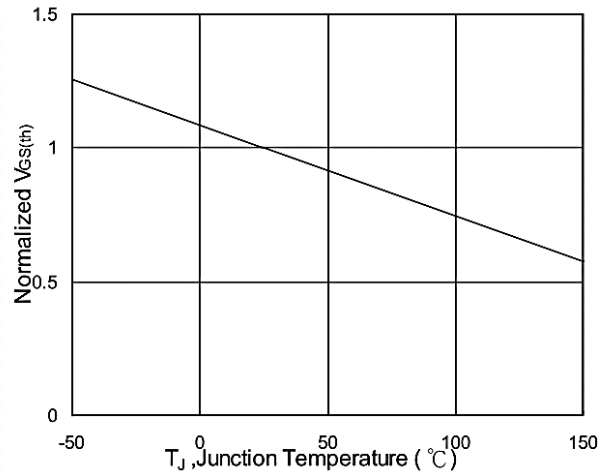


Fig.5 Normalized V_{GS} v.s T_J

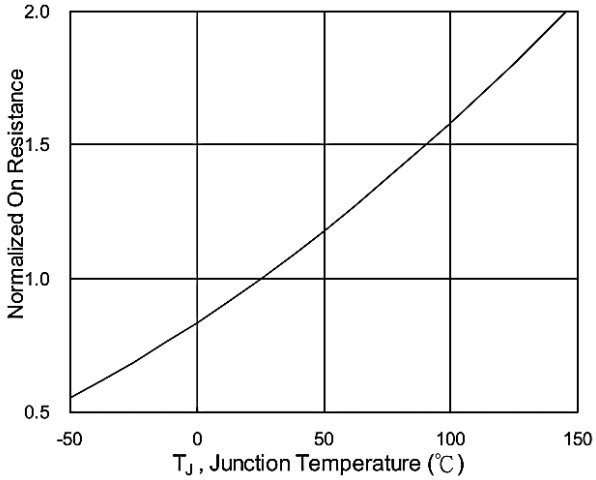


Fig.6 Normalized R_{DSON} v.s T_J

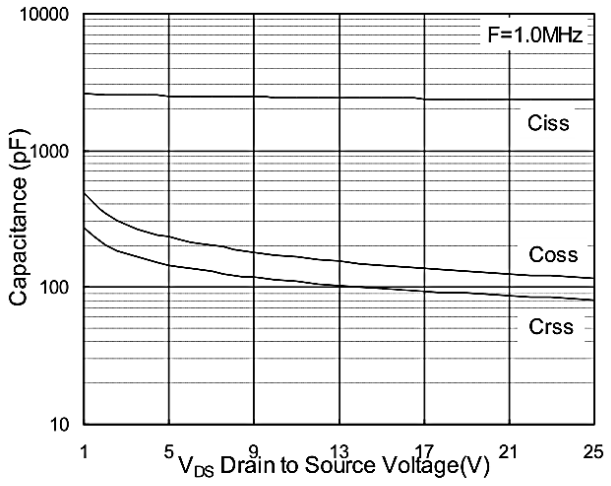


Fig.7 Capacitance

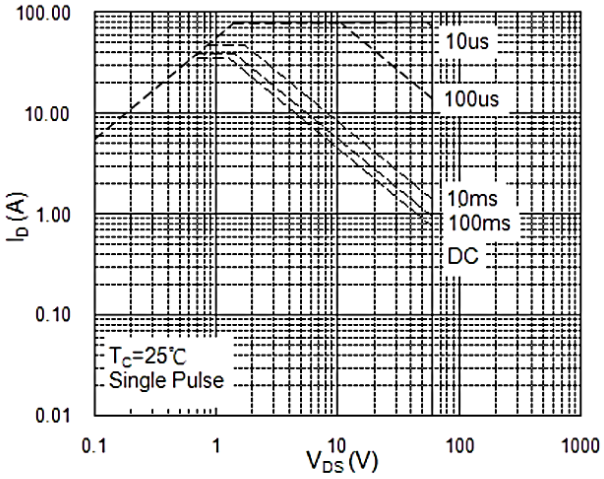


Fig.8 Safe Operating Area

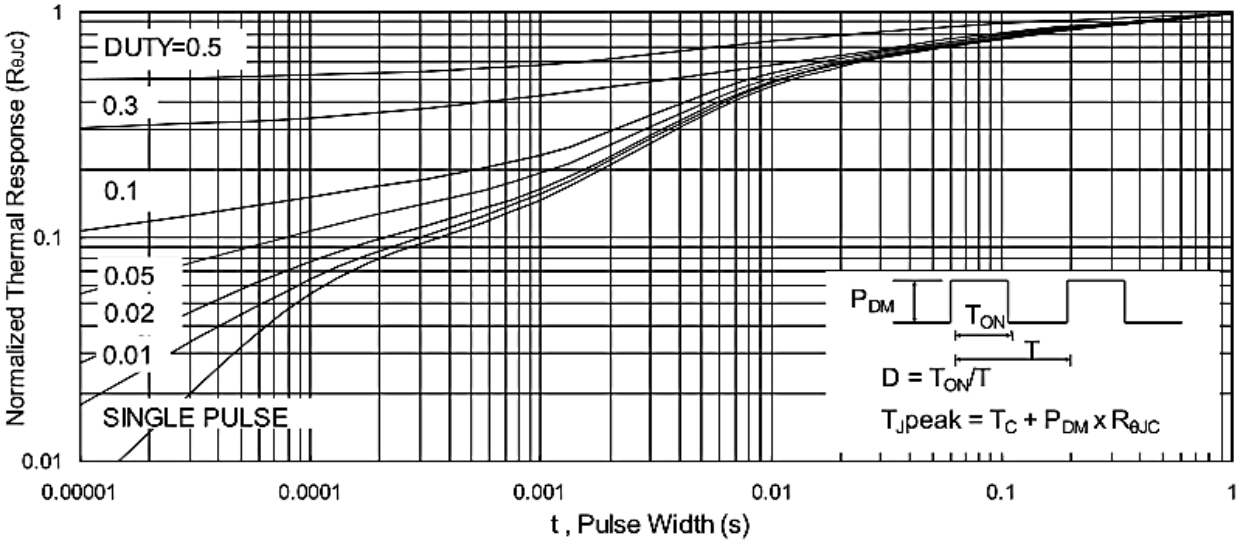


Fig.9 Normalized Maximum Transient Thermal Impedance

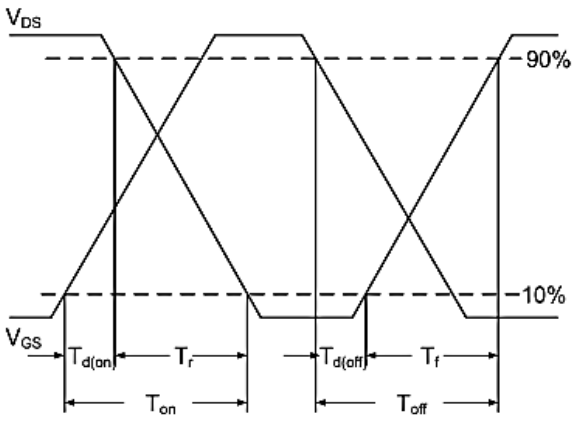


Fig.10 Switching Time Waveform

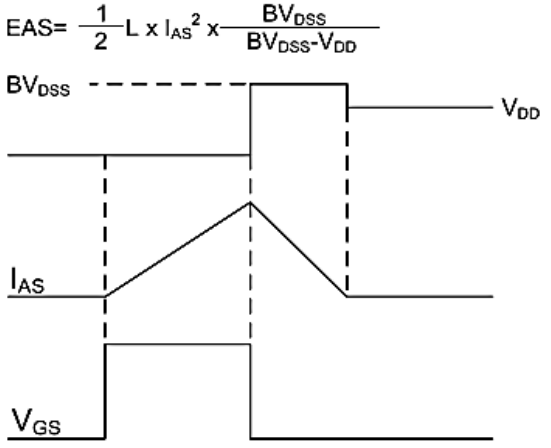
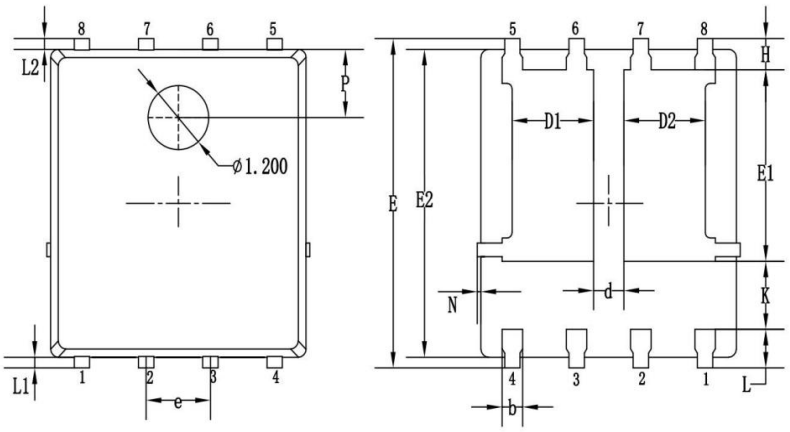
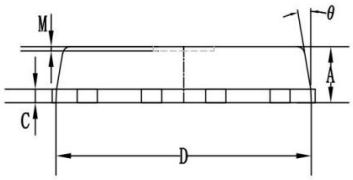


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-PDFN5*6-8L Single





Symbol	Dim in mm		
	min	tpy	max
A	0.9	1.05	1.2
b	0.3	0.4	0.5
C	0.2	0.25	0.35
D	4.9	5.05	5.2
D1	3.72	3.82	4.12
E	5.9	6.1	6.3
E1	2.34	2.44	2.54
E2	5.6	5.75	5.9
E3	0.67	0.77	0.87
e		1.27BSC	
H1	0.37	0.47	0.57
H2	0.33	0.43	0.53
K1	0.69	0.79	0.98
K2	0.65	0.75	0.85
L	0.54	0.74	0.84
L1/L2	0.1	0.2	0.3
θ	8°	10°	12°
M		0.08REF	
N	0		0.15
P		1.28REF	

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60V N+N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2020/12/1	Initial release