

30V N+P-Channel Enhancement Mode MOSFET

Description

The AP4606A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 30V$ $I_D = 8.8A$

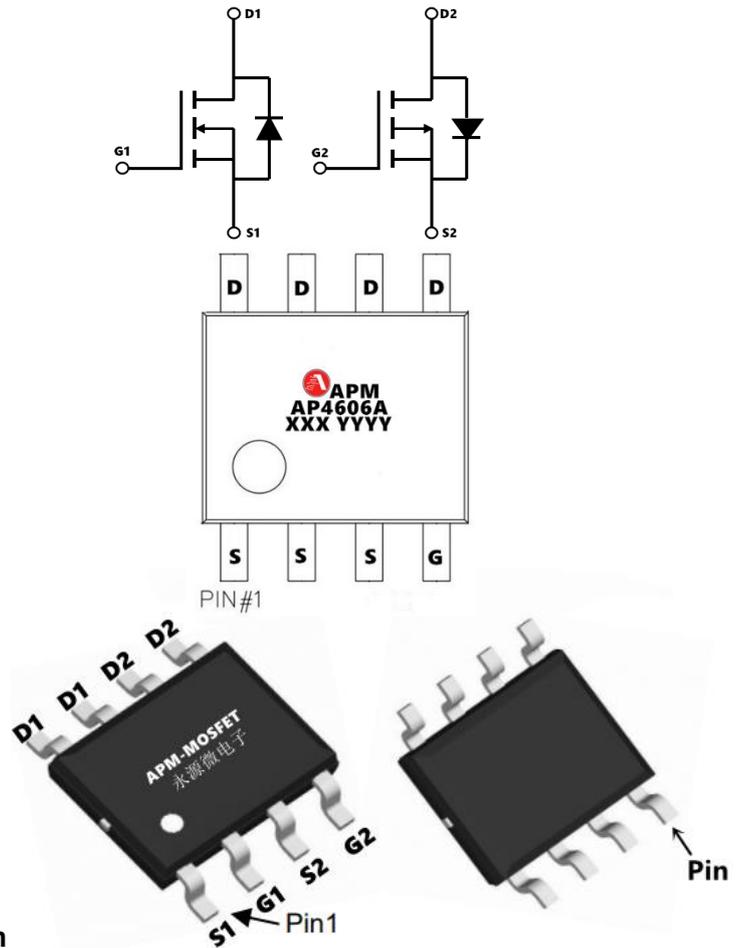
$R_{DS(ON)} < 22m\Omega$ @ $V_{GS}=10V$ (Type: 15m Ω)

$V_{DS} = -30V$ $I_D = -7.8A$

$R_{DS(ON)} < 45m\Omega$ @ $V_{GS}=-10V$ (Type: 35m Ω)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP4606A	SOP-8L	AP4606A XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.8	-7.8	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	5.5	-4.8	A
IDM	Pulsed Drain Current ²	24	-24	A
EAS	Single Pulse Avalanche Energy ³	26.6	37	mJ
IAS	Avalanche Current	12.7	10	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	1.5	1.5	W
TSTG	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85		$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	60		$^\circ\text{C}/\text{W}$

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N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	34	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.023	---	V/ $^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=5A$	---	15	22	m Ω
		$V_{GS}=4.5V, I_D=3A$	---	24	40	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=6A$	---	5.8	---	S
R _g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.3	---	Ω
Q _g	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=6A$	---	5	---	nC
Q _{gs}	Gate-Source Charge		---	1.11	---	
Q _{gd}	Gate-Drain Charge		---	2.61	---	
Td(on)	Turn-On Delay Time	$V_{DD}=12V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=6A$	---	7.7	---	ns
T _r	Rise Time		---	46	---	
Td(off)	Turn-Off Delay Time		---	11	---	
T _f	Fall Time		---	3.6	---	
C _{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	416	---	pF
C _{oss}	Output Capacitance		---	62	---	
Crss	Reverse Transfer Capacitance		---	51	---	
I _s	Continuous Source Current ^{1,6}	$V_G=V_D=0V, \text{Force Current}$	---	---	6.2	A
ISM	Pulsed Source Current ^{2,6}		---	---	24	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-32	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.02	---	V/ $^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-4.1A$	---	35	45	m Ω
		$V_{GS}=-4.5V, I_D=-3.5A$	---	48	60	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.7	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.32	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	---	4.7	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	24	---	Ω
Qg	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-5A$	---	5.22	---	nC
Qgs	Gate-Source Charge		---	1.25	---	
Qgd	Gate-Drain Charge		---	2.3	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-1A$	---	18.4	---	ns
Tr	Rise Time		---	11.4	---	
Td(off)	Turn-Off Delay Time		---	39.4	---	
Tf	Fall Time		---	5.2	---	
Ciss	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	463	---	pF
Coss	Output Capacitance		---	82	---	
Crss	Reverse Transfer Capacitance		---	68	---	
Is	Continuous Source Current ^{1,6}	$V_G=V_D=0V, \text{Force Current}$	---	---	-4	A
ISM	Pulsed Source Current ^{2,6}		---	---	-24	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

- 1、The data tested by surface mounted on a 1 inch FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\cong 300\mu\text{s}$, duty cycle $\cong 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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N-Channel Typical Characteristics

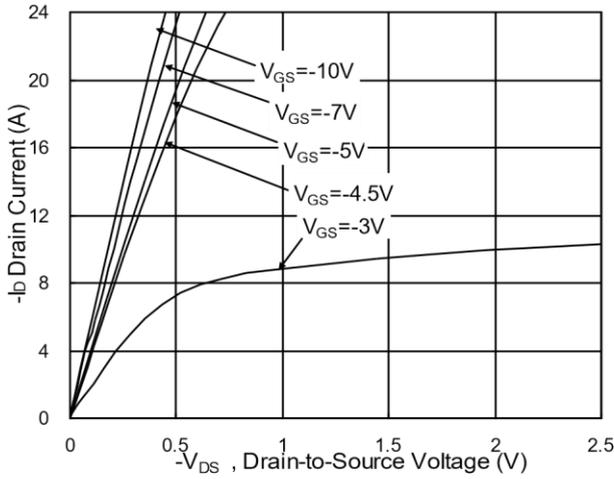


Fig.1 Typical Output Characteristics

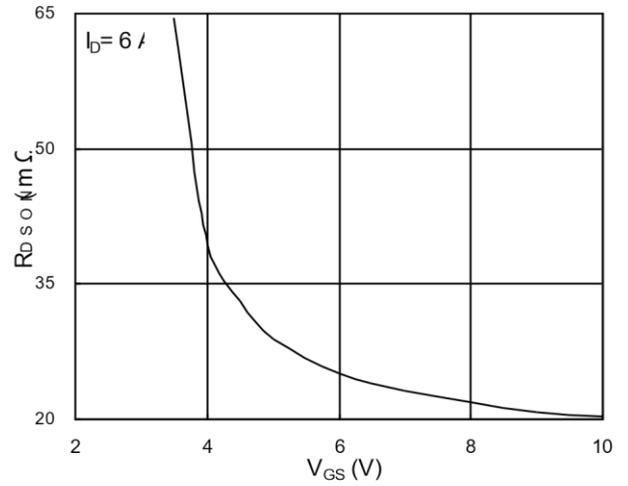


Fig.2 On-Resistance vs. Gate-Source

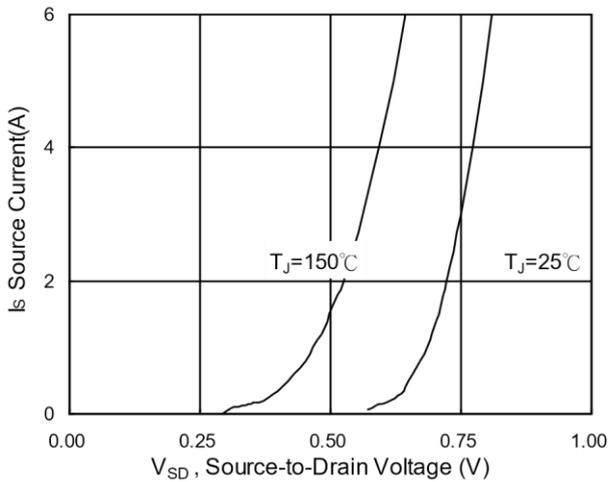


Fig.3 Forward Characteristics Of Reverse

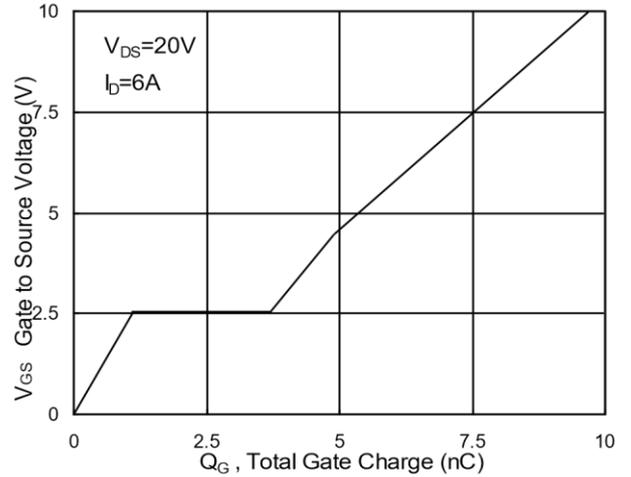


Fig.4 Gate-Charge Characteristics

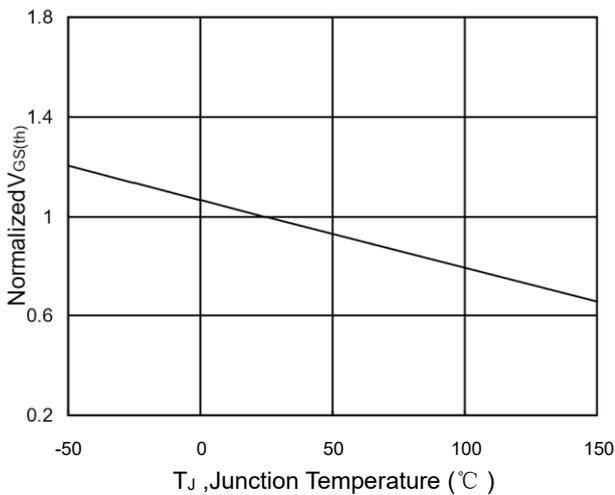


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

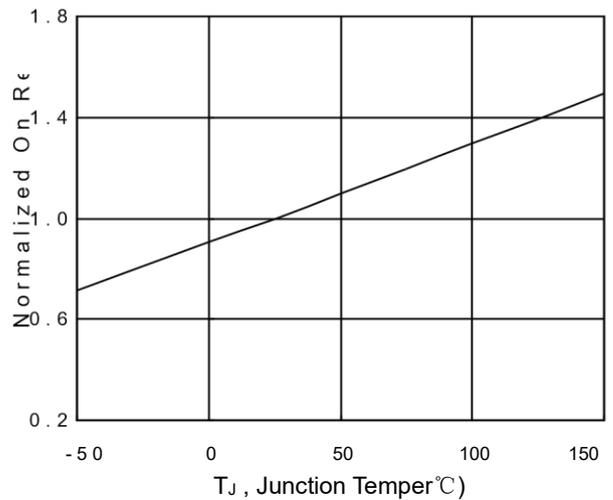


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



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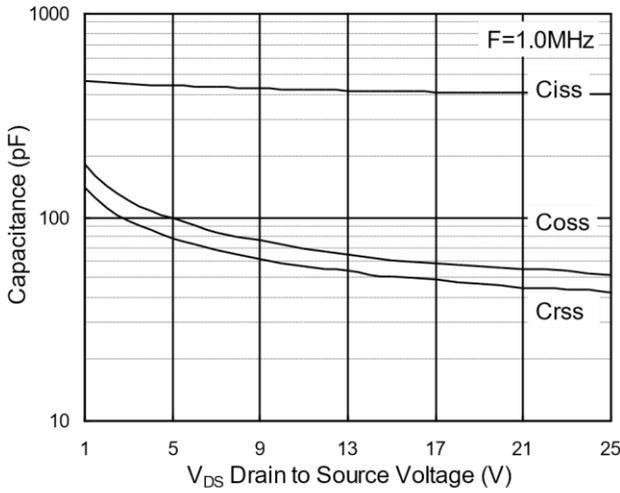


Fig.7 Capacitance

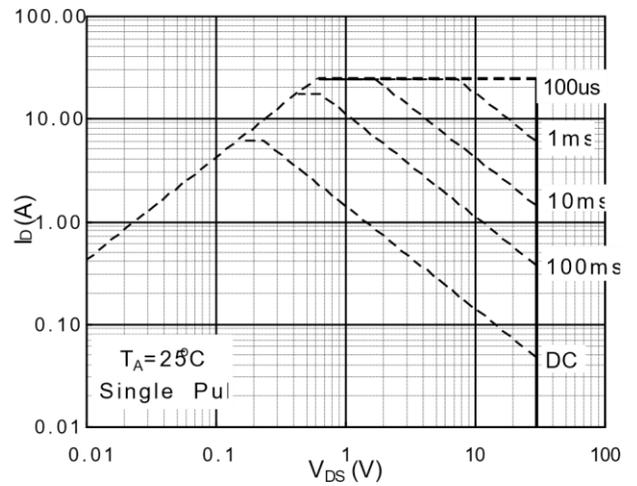


Fig.8 Safe Operating Area

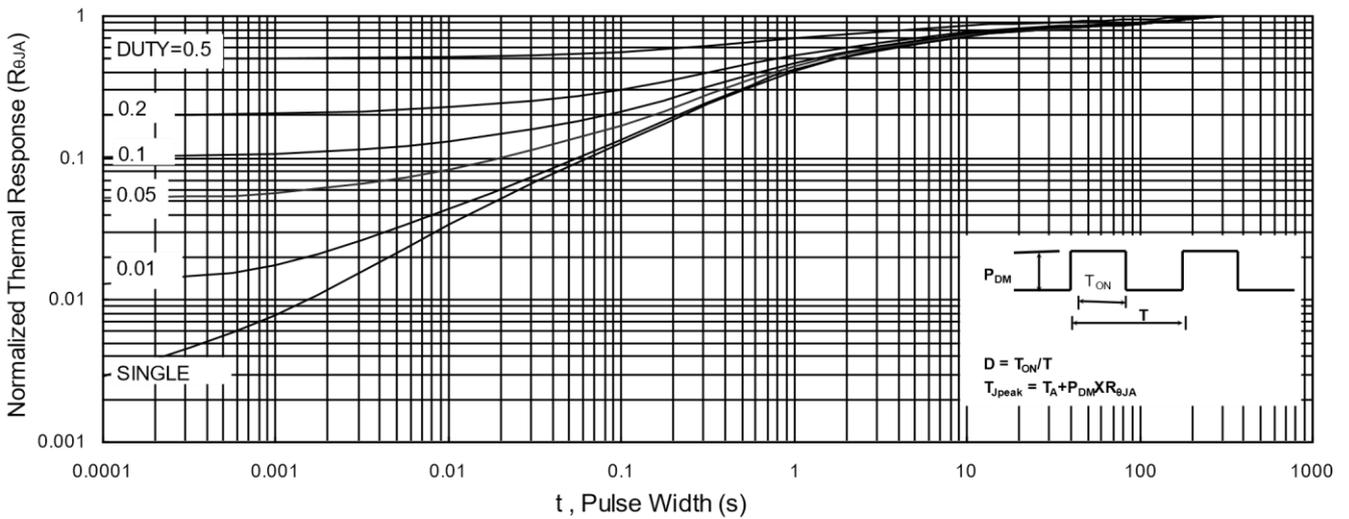


Fig.9 Normalized Maximum Transient Thermal Impedance

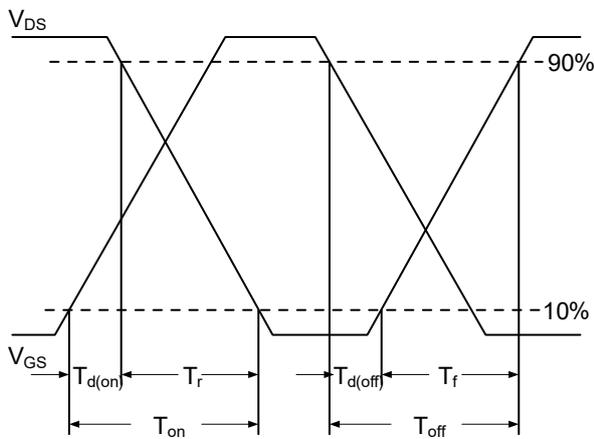


Fig.10 Switching Time Waveform

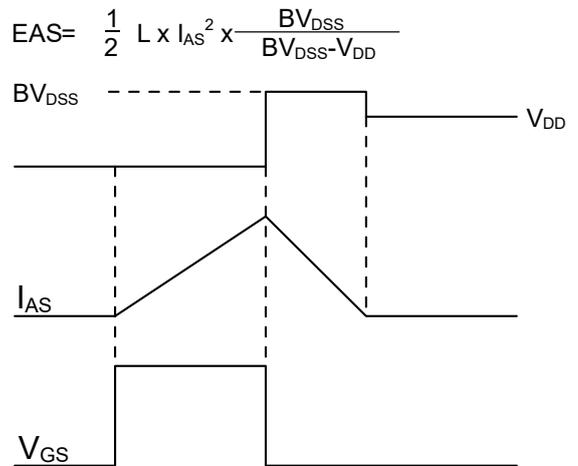


Fig.11 Unclamped Inductive Switching Waveform

P-Channel Typical Characteristics

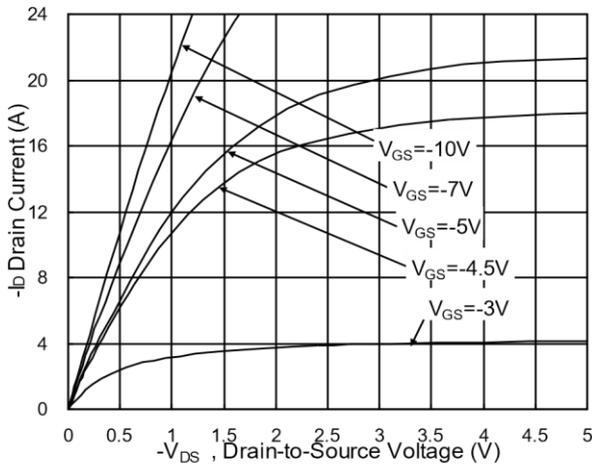


Fig.1 Typical Output Characteristics

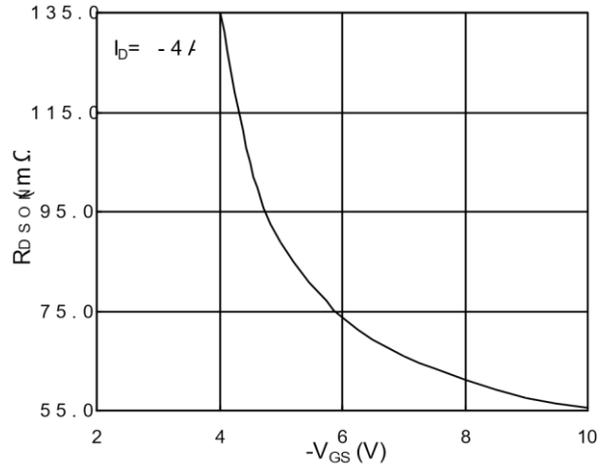


Fig.2 On-Resistance vs. G-S Voltage

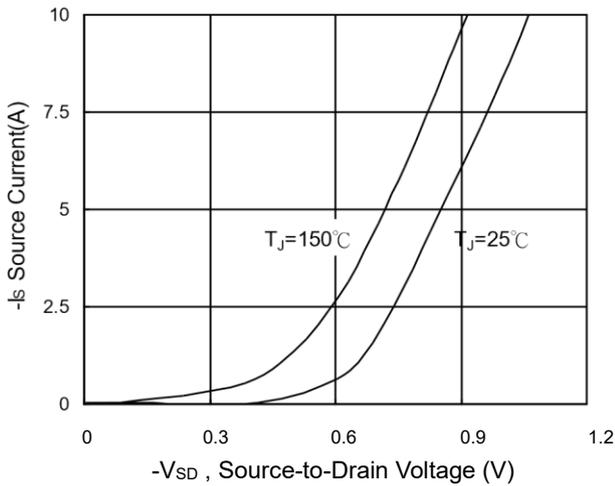


Fig.3 Forward Characteristics of Reverse

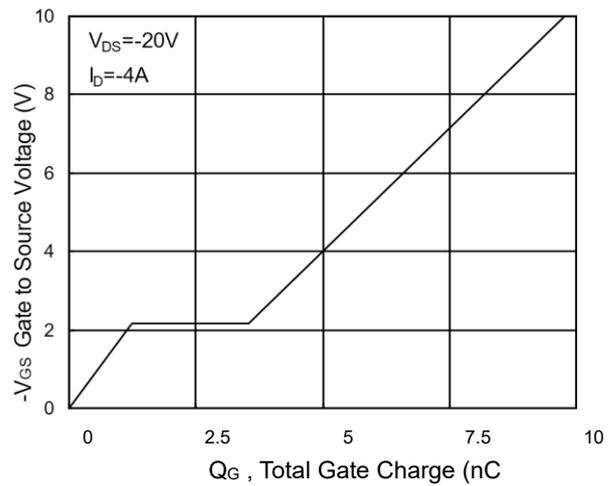


Fig.4 Gate-Charge Characteristics

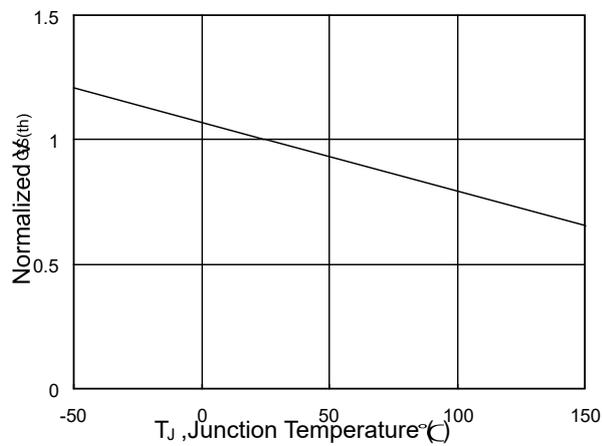


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

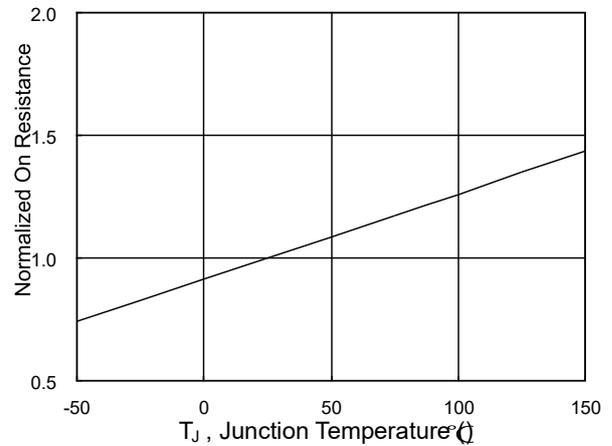


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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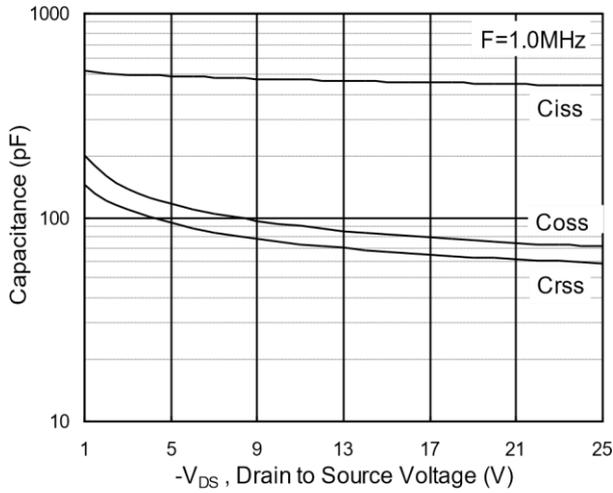


Fig.7 Capacitance

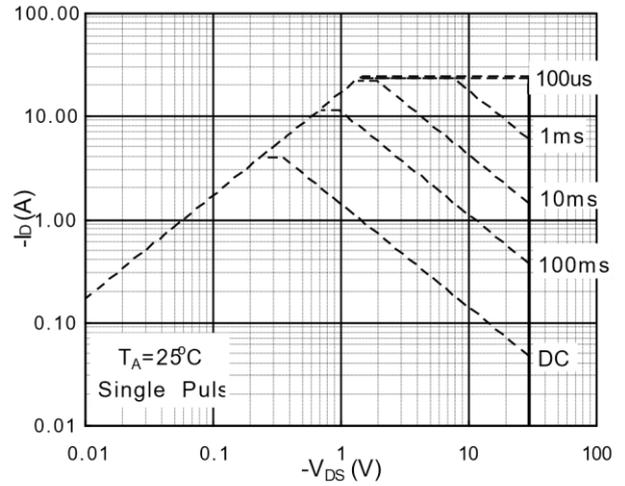


Fig.8 Safe Operating Area

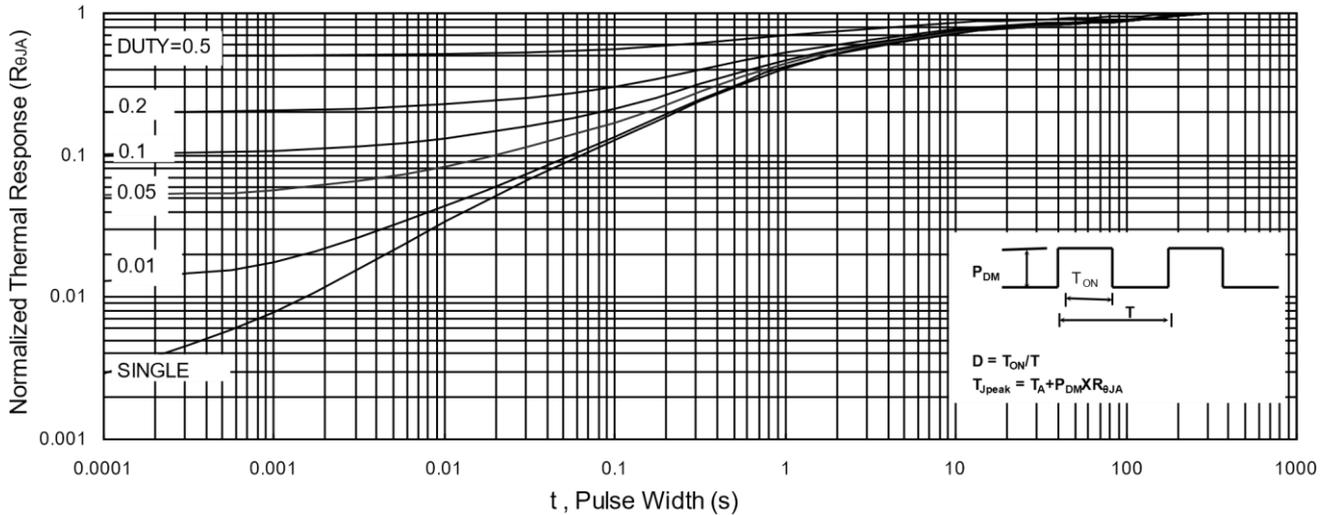


Fig.9 Normalized Maximum Transient Thermal Impedance

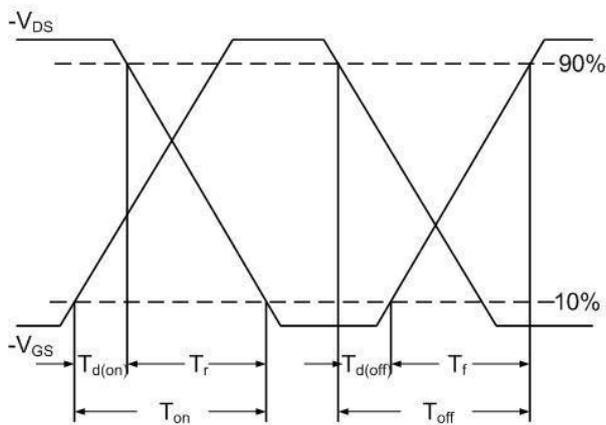


Fig.10 Switching Time Waveform

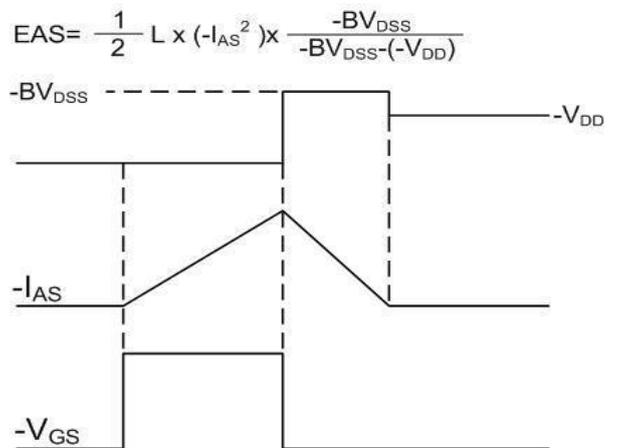
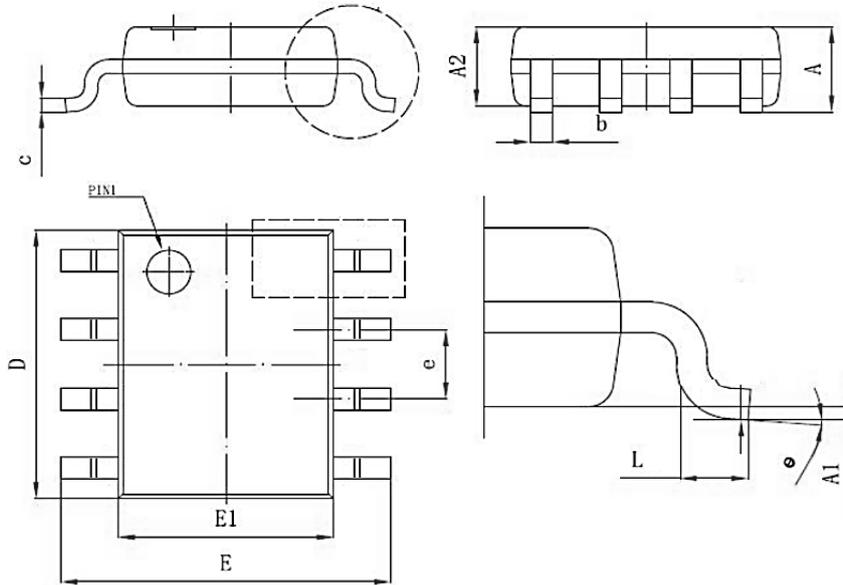


Fig.11 Unclamped Inductive Switching Waveform

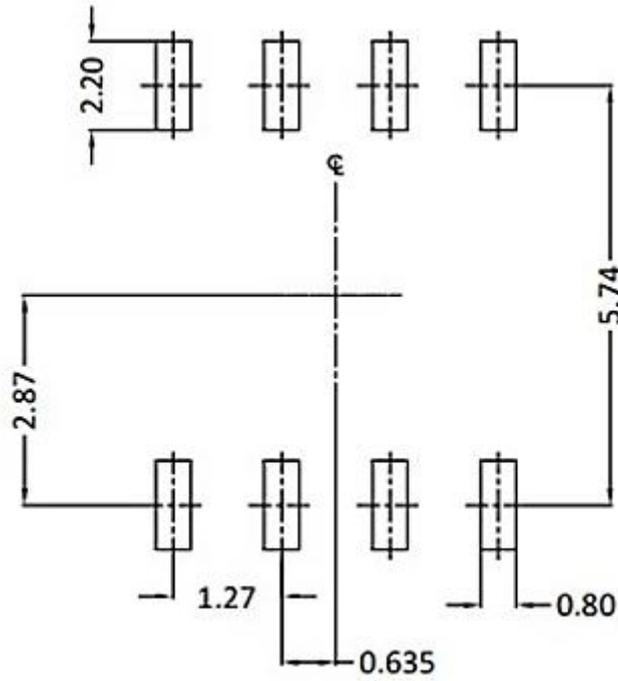


Package Mechanical Data-SOP-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	1.35	1.55	1.75
A1	0.02	0.15	0.25
A2	1.425	1.45	1.475
b	0.3	0.4	0.5
c	0.15	0.2	0.25
D	4.8	5	5.2
E	5.8	6	6.2
E1	3.8	4	4.2
e	1.27BSC		
L	0.4		1.27
θ	0°		8°

Recommended Minimum Pads



Dimensions in (mm)

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Edition	Date	Change
REV1.0	2022/12/10	Initial release
REV1.1	2024/3/1	Reduce RDS(on)

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