

## 60V N-Channel Enhancement Mode MOSFET

### Description

The AP40N06DF uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 60V$   $I_D = 40A$

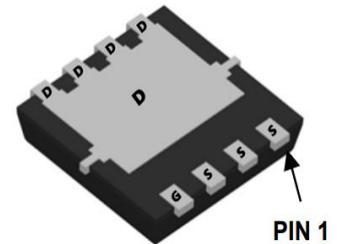
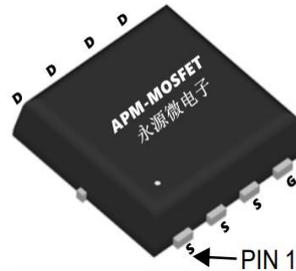
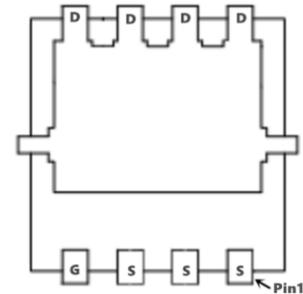
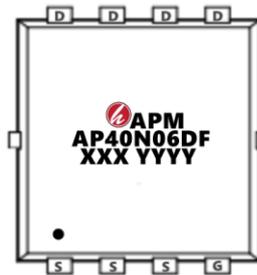
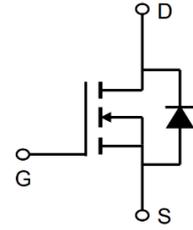
$R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=10V$  (Type: 20m $\Omega$ )

### Application

Battery protection

Load switch

Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP40N06DF	PDFN3*3-8L	AP40N06DF XXXX YYYY	5000

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	40	A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	18	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	114	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	25.5	mJ
$I_{AS}$	Avalanche Current	22	A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	34.7	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	85	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	3.6	$^\circ\text{C/W}$

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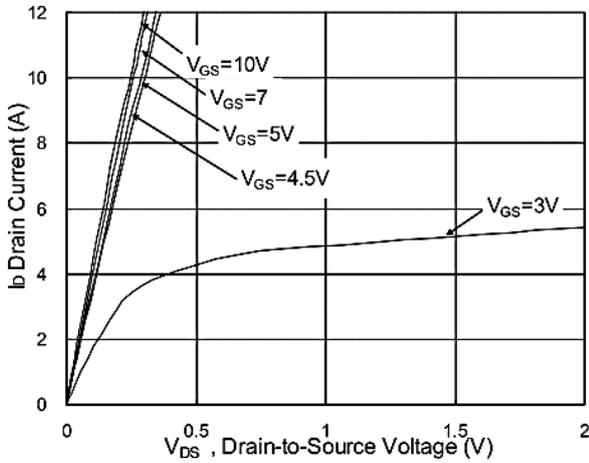
### Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	65	---	V
ΔBVDSS/ΔTJ	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.063	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A	---	20	32	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	30	38	
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.6	2.5	V
ΔVGS(th)	V <sub>GS(th)</sub> Temperature Coefficient		---	-5.24	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =15A	---	17	---	S
Rg	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	3.2	---	Ω
Qg	Total Gate Charge (4.5V)	V <sub>DS</sub> =48V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =12A	---	12.6	---	nC
Qgs	Gate-Source Charge		---	3.2	---	
Qgd	Gate-Drain Charge		---	6.3	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V , R <sub>G</sub> =3.3Ω, I <sub>D</sub> =10A	---	8	---	ns
T <sub>r</sub>	Rise Time		---	14.2	---	
Td(off)	Turn-Off Delay Time		---	24.4	---	
T <sub>f</sub>	Fall Time		---	4.6	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	1378	---	pF
C <sub>oss</sub>	Output Capacitance		---	86	---	
Crss	Reverse Transfer Capacitance		---	64	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	23	A
ISM	Pulsed Source Current <sup>2,5</sup>		---	---	46	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

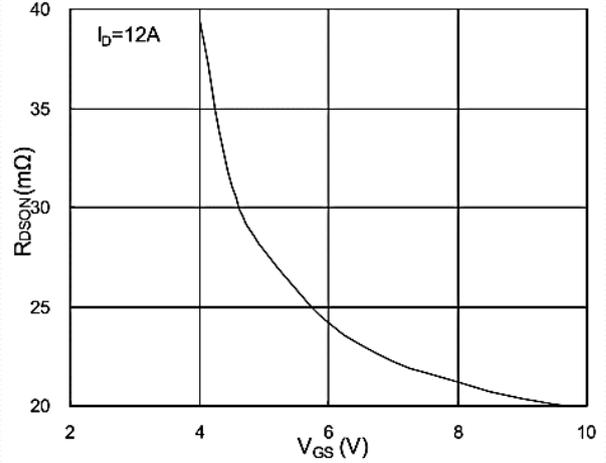
**Note :**

- 1、The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The EAS data shows Max. rating. The test condition is VDD=25V, VGS=10V, L=0.1mH, IAS=22A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

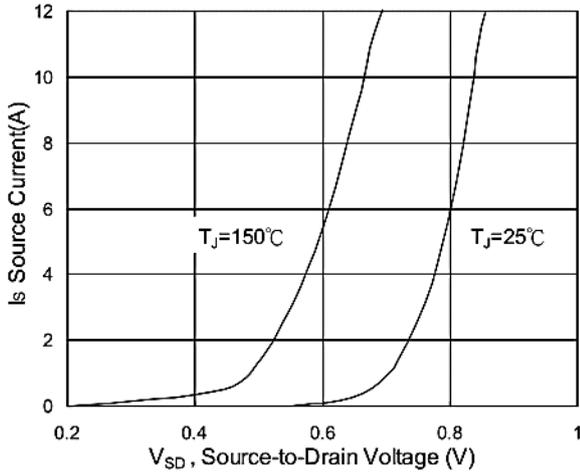
**Typical Characteristics**



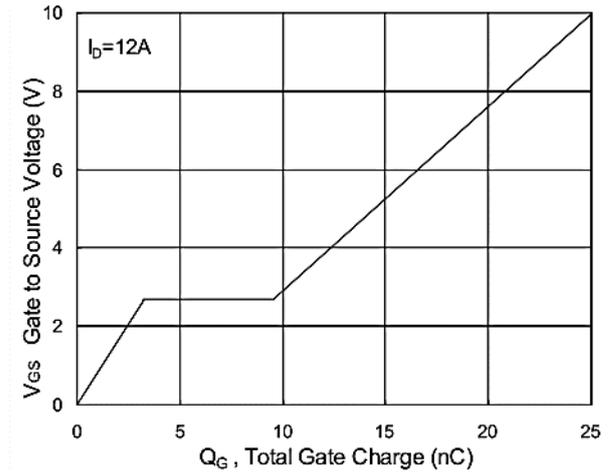
**Fig.1 Typical Output Characteristics**



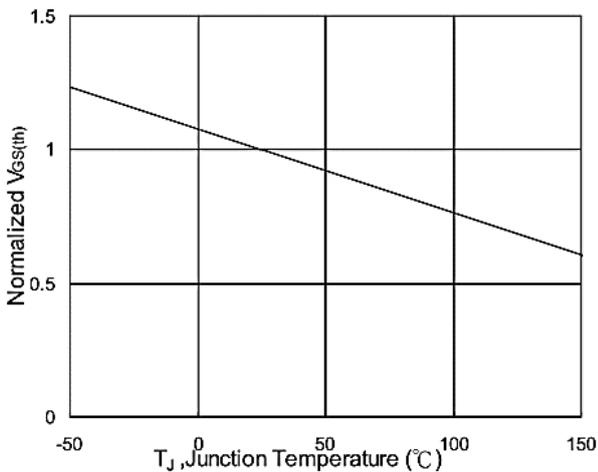
**Fig.2 On-Resistance v.s Gate-Source**



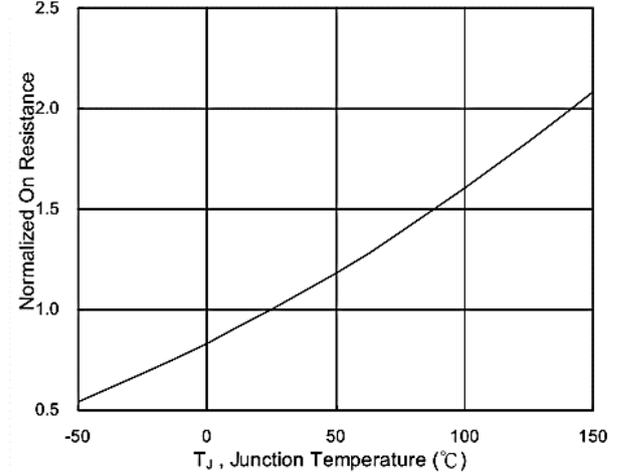
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

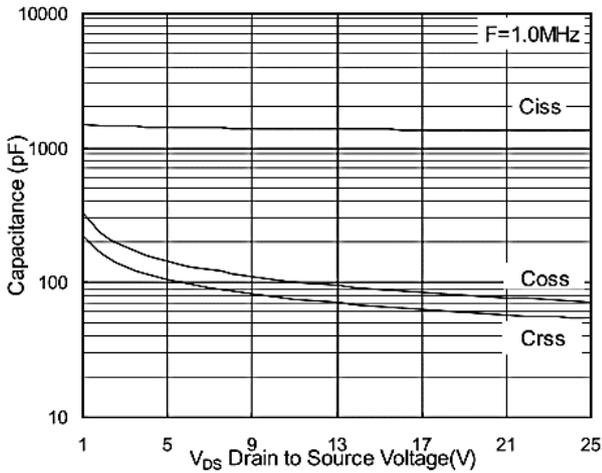


**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**

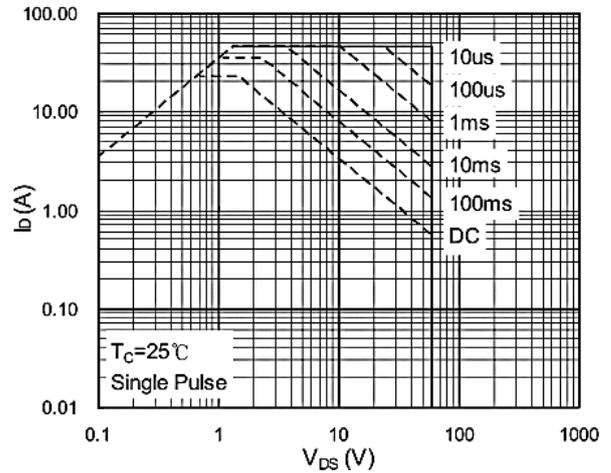


**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**

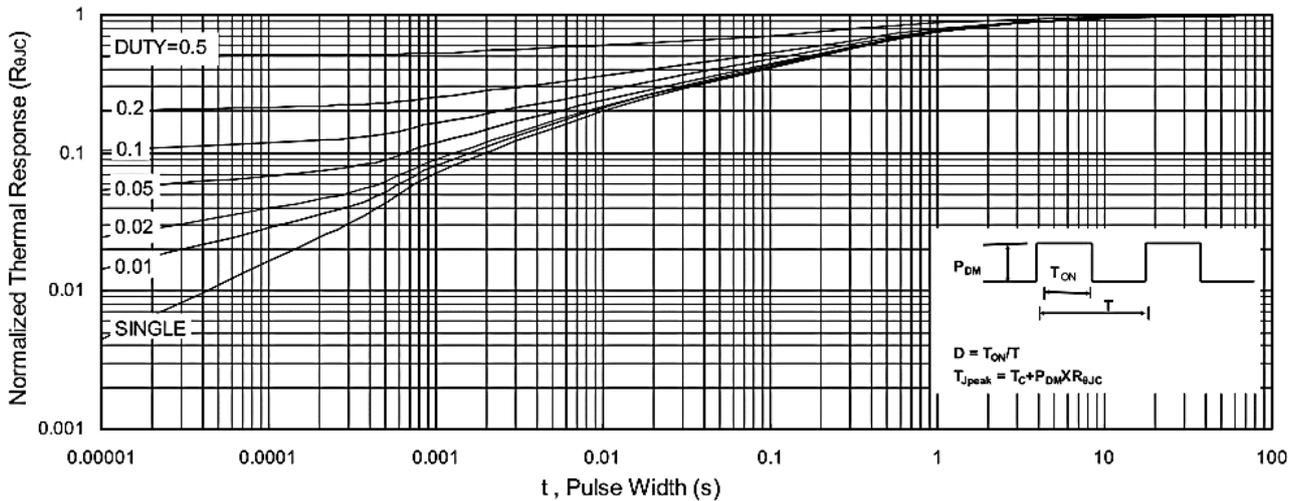
**60V N-Channel Enhancement Mode MOSFET**



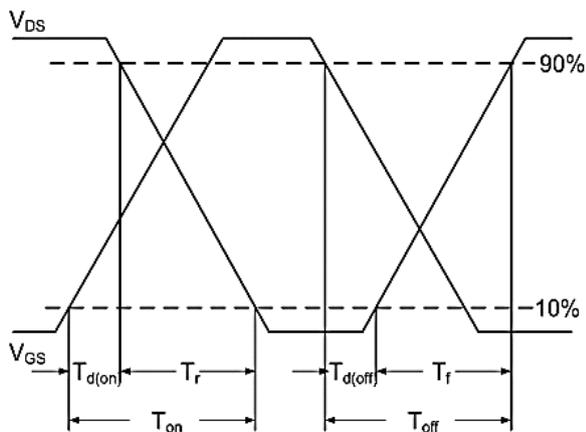
**Fig.7 Capacitance**



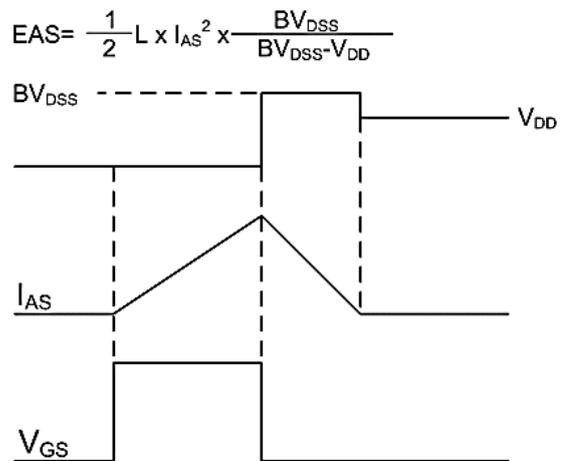
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

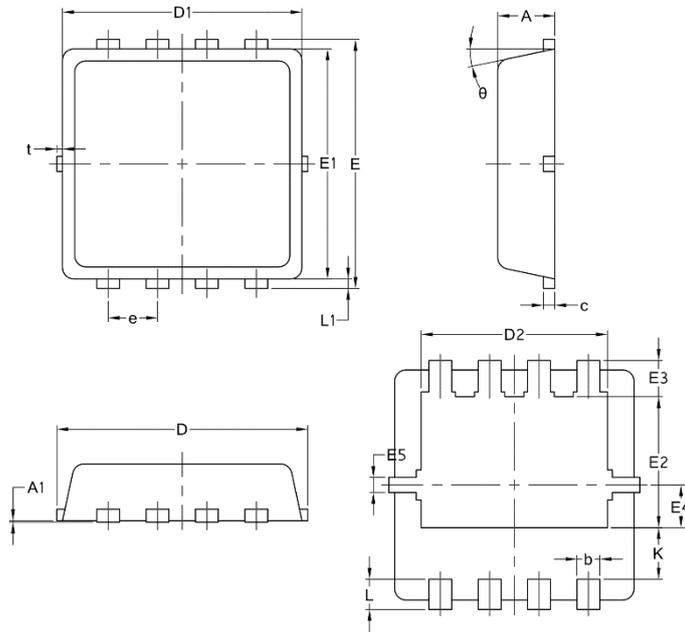


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

### Package Mechanical Data-DFN3\*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14

**60V N-Channel Enhancement Mode MOSFET****Attention**

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Edition	Date	Change
Rve3.8	2018/1/23	Initial release

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