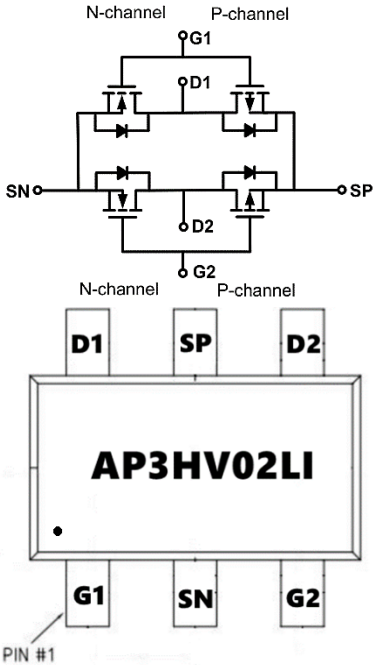
AP3HV02LI

20V NP+NP-Channel Enhancement Mode MOSFET

Description

The AP3HV02LI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 20V I_D =3.3A

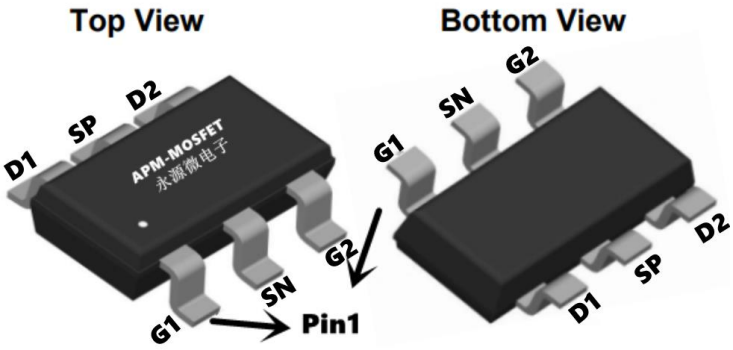
$R_{DS(ON)}$ < 50mΩ @ V_{GS}=4.5V （**Type：42mΩ**）

V_{DS} = -20V I_D =-2.8A

$R_{DS(ON)}$ < 120mΩ @ V_{GS}=-4.5V（**Type：95mΩ**）

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3HV02LI	SOT23-6L	AP3HV02LI	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	3.3	-2.8	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	1.5	-1.0	A
I_{DM}	Pulsed Drain Current[2]	52	-40	A
EAS	Single Pulse Avalanche Energy[3]	12	18	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	1.5	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	105		℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	50		℃/W

N-Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20	22	---	V
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=3A	---	42	50	mΩ
		V_{GS}=2.5V , I_D=2A	---	55	65	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.4	0.6	1.2	V
IDSS	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=16V , V_{GS}=0V , T_J=55℃	---	---	5	
IGSS	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=3A	---	10.5	---	S
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=4.5V , I_D=3A	---	4.6	---	nC
Qgs	Gate-Source Charge		---	0.7	---	
Qgd	Gate-Drain Charge		---	1.5	---	
Td(on)	Turn-On Delay Time	V_{DD}=10V , V_{GS}=4.5V , R_G=3.3Ω I_D=3A	---	1.6	---	ns
T_r	Rise Time		---	42	---	
Td(off)	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	7	---	
Ciss	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	310	---	pF
Coss	Output Capacitance		---	49	---	
Crss	Reverse Transfer Capacitance		---	35	---	
IS	Continuous Source Current[1,4]	V_G=V_D=0V , Force Current	---	---	3.6	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D= -250μA	-20	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} = -20V, V_{GS} = 0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V_{DS} =0V, V_{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D= -250μA	-0.4	-0.7	-1.0	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS} =-4.5V, I_D =-2A	-	95	120	mΩ
		V_{GS} =-2.5V, I_D =-1A	-	135	190	
Ciss	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz	-	185	-	pF
Coss	Output Capacitance		-	35	-	pF
Crss	Reverse Transfer Capacitance		-	25	-	pF
Q_g	Total Gate Charge	V_{DS} = -10V, I_D = -2A, V_{GS} = -4.5V	-	2.2	-	nC
Qgs	Gate-Source Charge		-	0.5	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	0.5	-	nC
td(on)	Turn-on Delay Time	V_{DD} = -10V, R_L=5Ω, R_{GEN}=3Ω,V_{GS}=-4.5V,	-	10	-	ns
tr	Turn-on Rise Time		-	30	-	ns
td(off)	Turn-off Delay Time		-	63	-	ns
t_f	Turn-off Fall Time		-	50	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-2.8	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-8	A
VSD	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S = -2A	-	-	-1.2	V

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

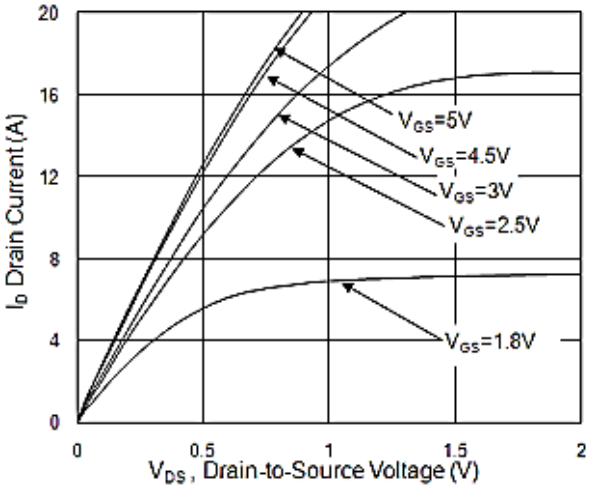


Fig.1 Typical Output Characteristics

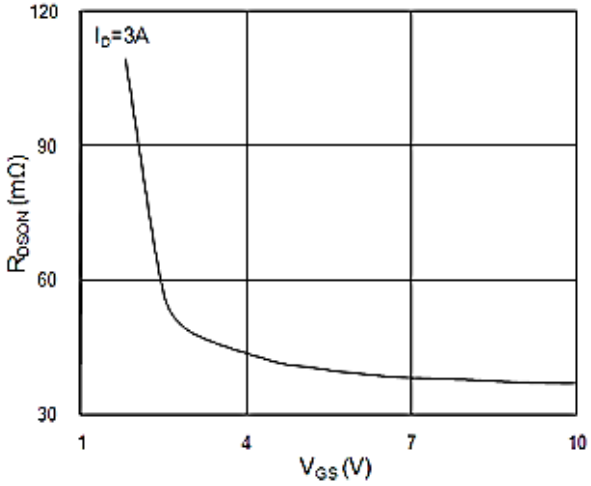
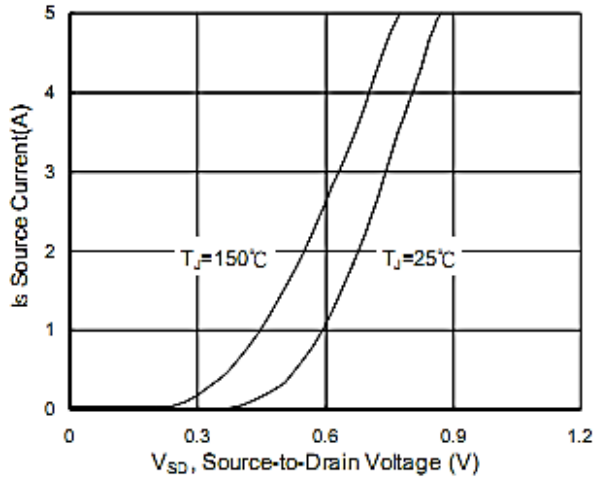
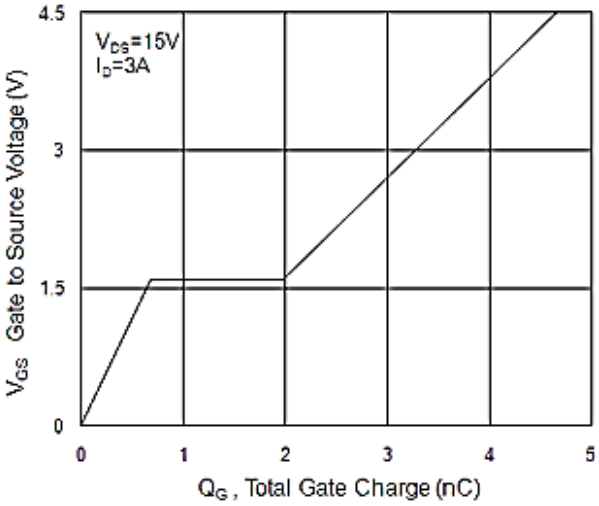


Fig.2 On-Resistance vs. G-S Voltage





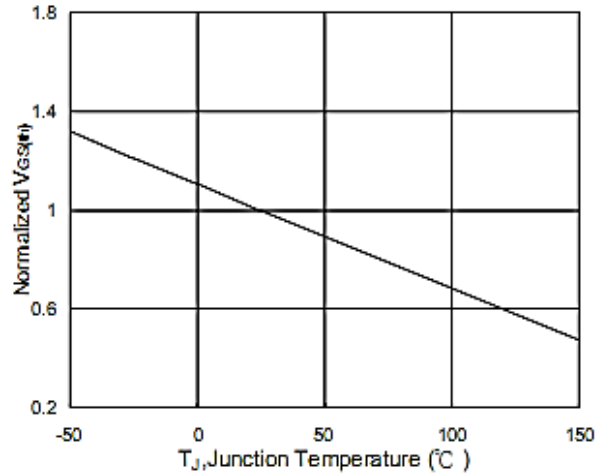


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

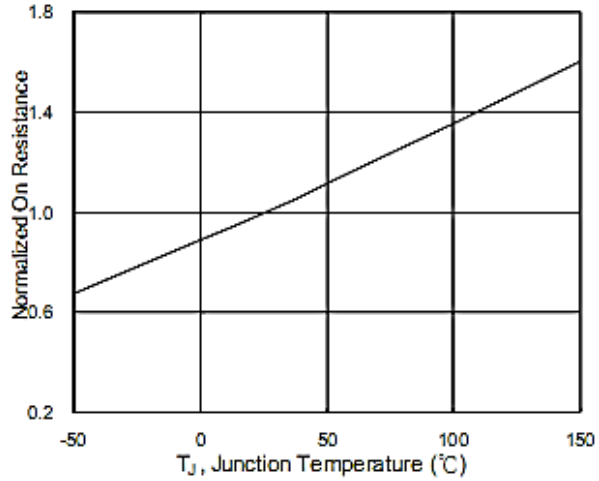


Fig.6 Normalized R_{DSON} vs. T_J

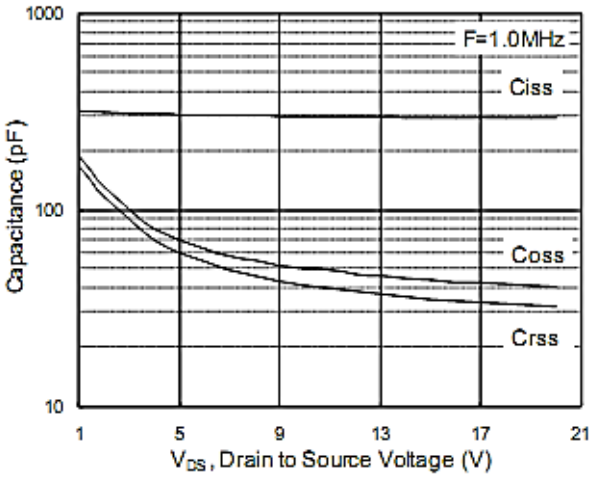


Fig.7 Capacitance

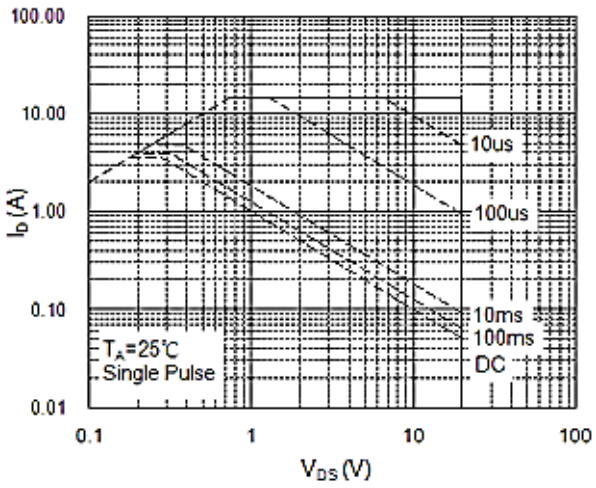


Fig.8 Safe Operating Area

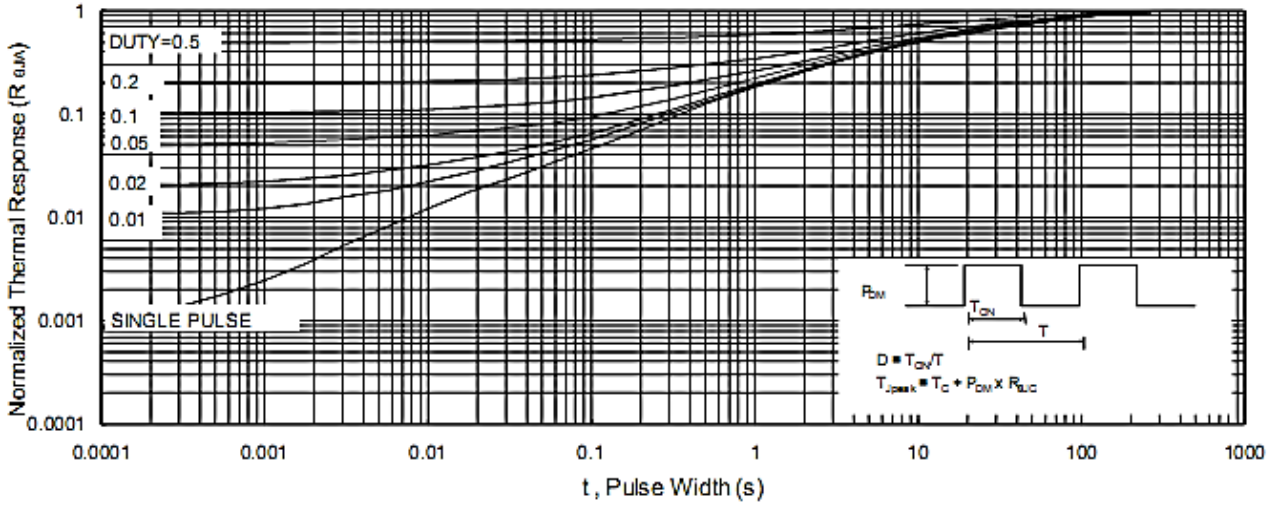


Fig.9 Normalized Maximum Transient Thermal Impedance

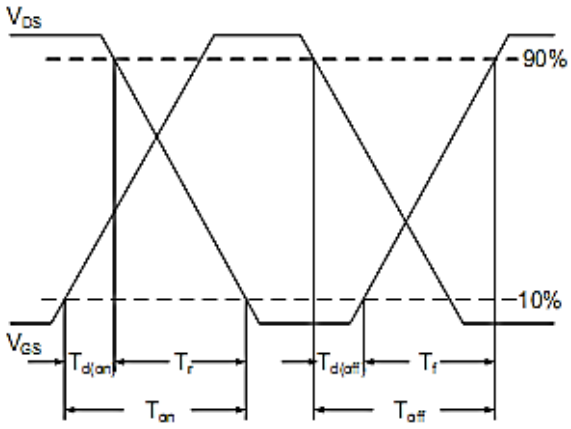


Fig.10 Switching Time Waveform

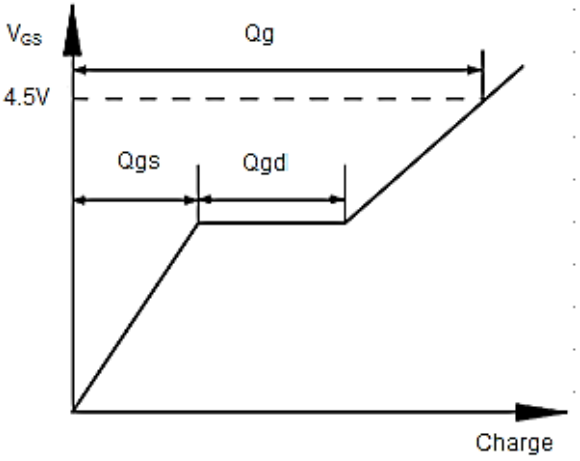


Fig.11 Gate Charge Waveform

P-Channel Typical Characteristics

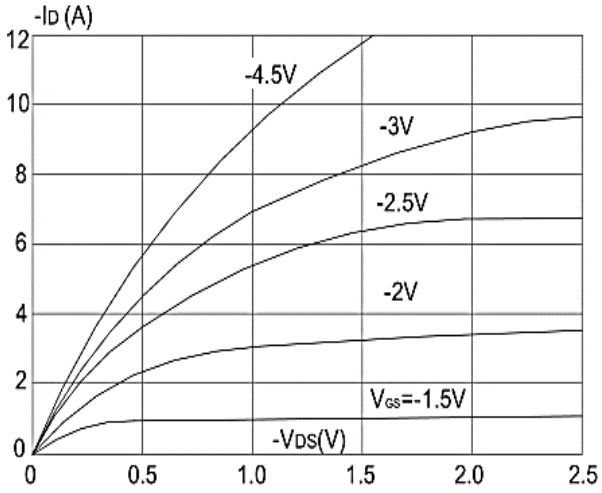


Figure1: Output Characteristics

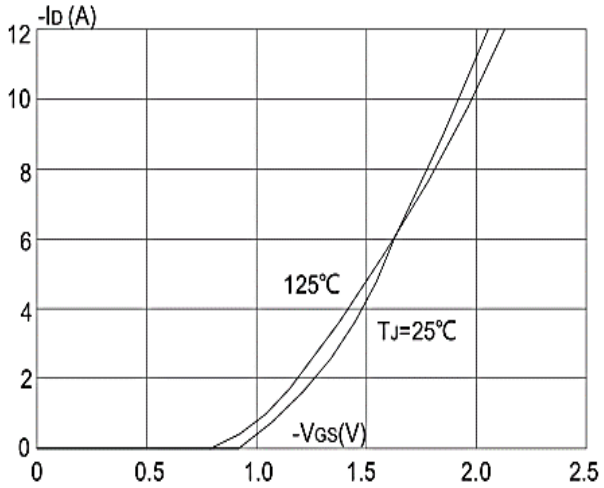


Figure 2: Typical Transfer Characteristics

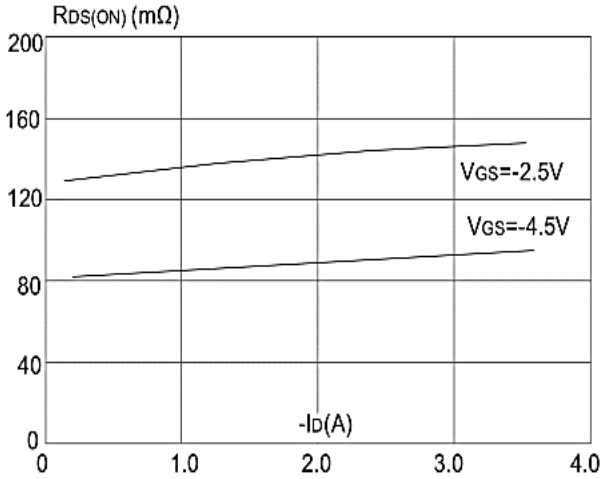


Figure 3:On-resistance vs. Drain Current

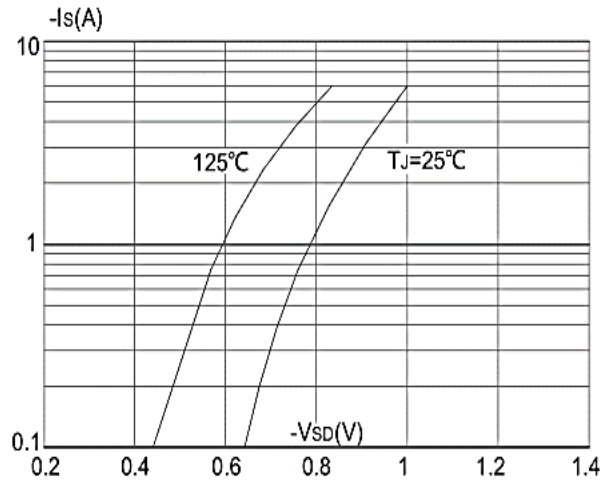


Figure 4: Body Diode Characteristics

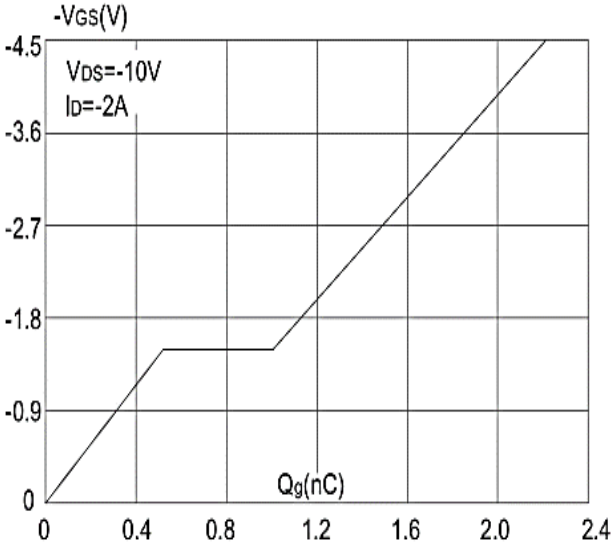


Figure 5: Gate Charge Characteristics

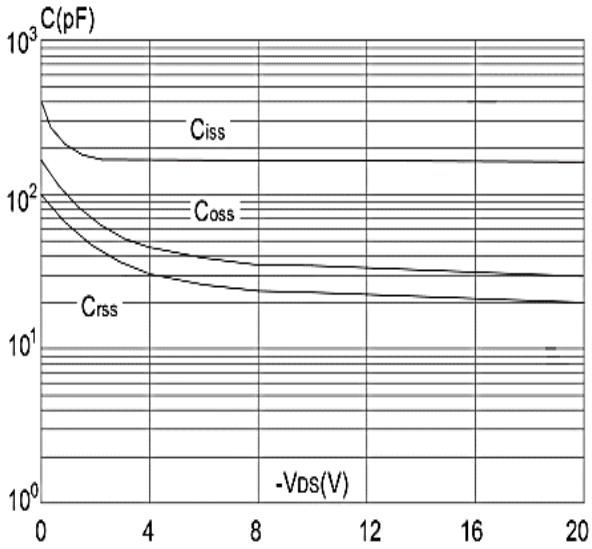


Figure 6: Capacitance Characteristics

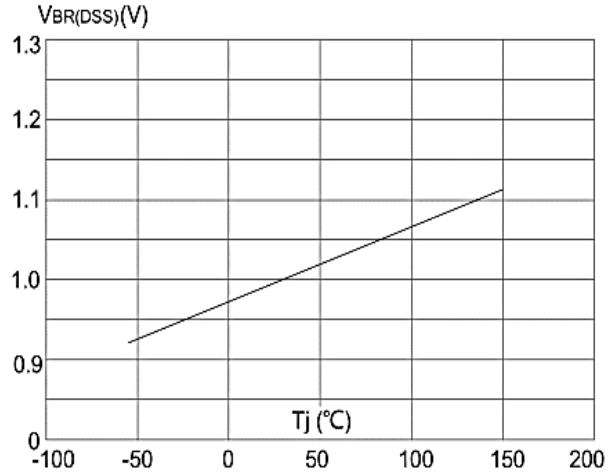


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

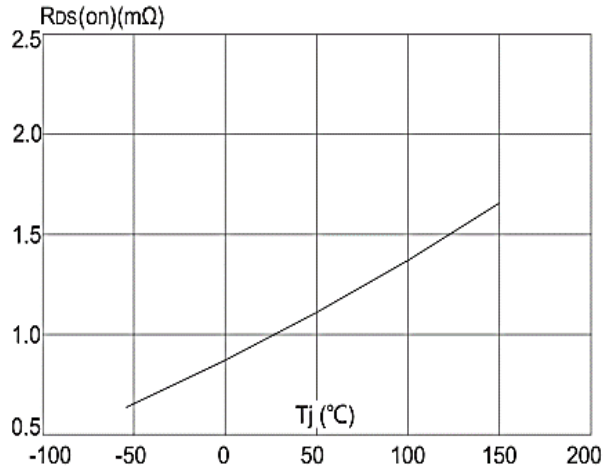


Figure 8: Normalized on Resistance vs. Junction Temperature

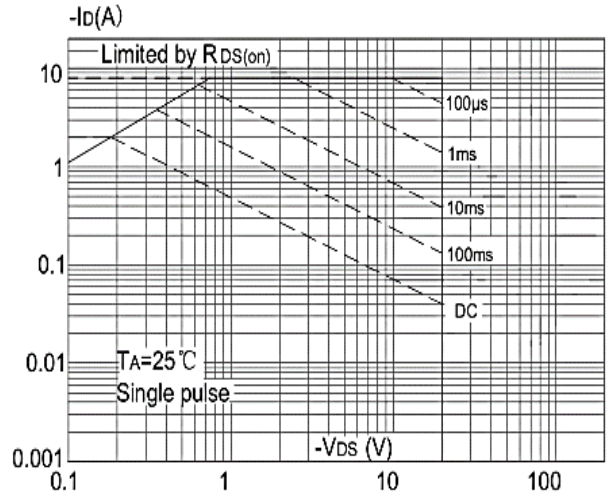


Figure 9: Maximum Safe Operating Area

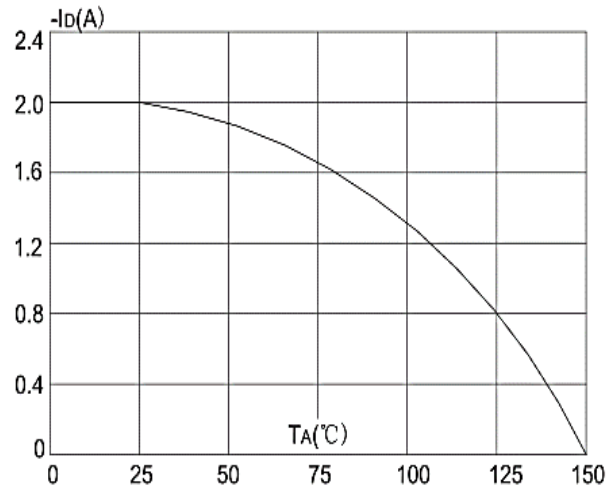


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

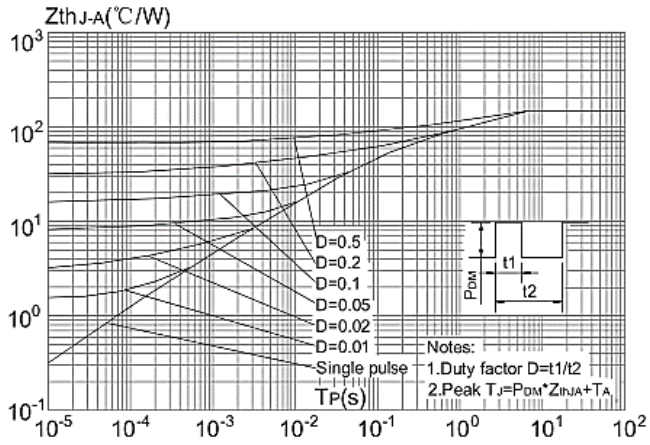
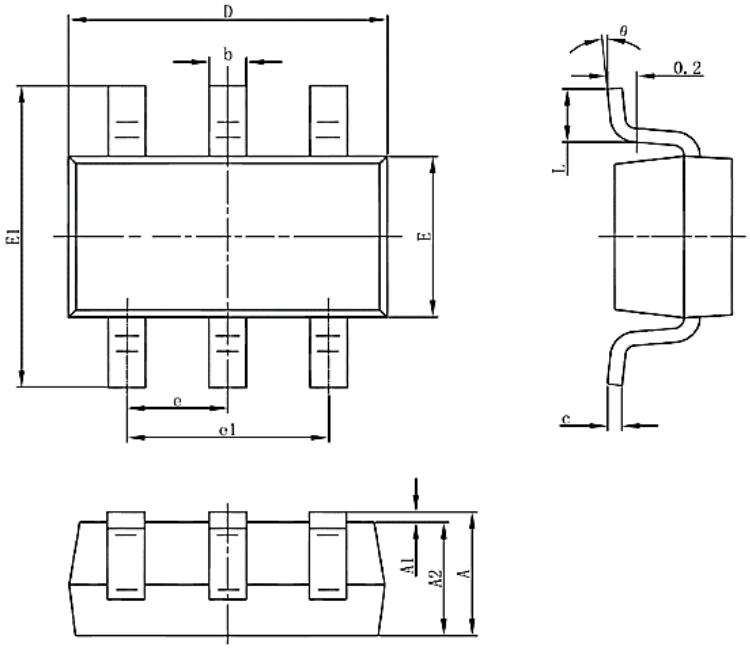


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

Package Mechanical Data-SOT23-6-Double



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950（BSC）		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0	8	0	8

Attention

1,Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.

2,APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.

3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design,and structural design.

5,In the event that any or all APM Microelectronics products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

6, No part of this publication may be reproduced or transmitted in any form or by any means,electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.

7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement,etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you Intend to use.

Edition	Date	Change
REV1.0	2021/12/21	Initial release