

60V N+P-Channel Enhancement Mode MOSFET

Description

The AP30G06GD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 60V$ $I_D = 36A$

$R_{DS(ON)} < 32m\Omega$ @ $V_{GS}=10V$ (Type: 25m Ω)

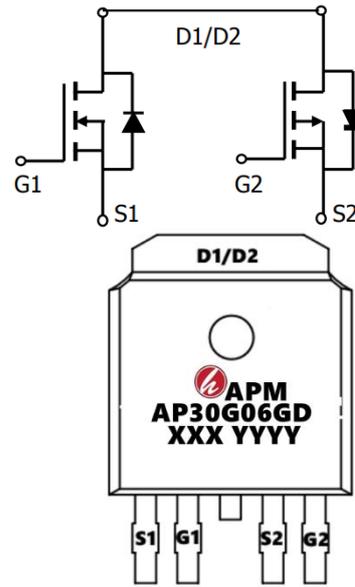
$V_{DS} = -60V$ $I_D = -29A$

$R_{DS(ON)} < 58m\Omega$ @ $V_{GS}=-10V$ (Type: 46m Ω)

Application

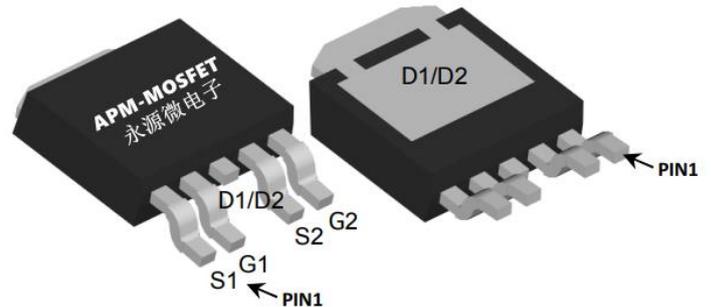
Boost driver

Brushless motor



Top View

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP30G06GD	TO-252-4L	AP30G06GD XXX YYYYY	2500

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	36	-29	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	15.8	-15.3	A
IDM	Pulsed Drain Current ²	105	-95	A
EAS	Single Pulse Avalanche Energy ³	125.5	135.3	mJ
IAS	Avalanche Current	22.6	-26.6	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation ⁴	1.5		W
TSTG	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62.5		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	3.6		$^\circ C/W$

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N-Channel Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	60	70	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.063	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =4A	---	25	36	mΩ
		V _{GS} =4.5V, I _D =2A	---	32	38	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.2	1.6	2.5	V
ΔVGS(th)	V _{GS(th)} Temperature Coefficient		---	-5.24	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =5V, I _D =4A	---	21	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	3.2	---	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =48V, V _{GS} =4.5V, I _D =4A	---	12.6	---	nC
Q _{gs}	Gate-Source Charge		---	3.2	---	
Q _{gd}	Gate-Drain Charge		---	6.3	---	
Td(on)	Turn-On Delay Time	V _{DD} =30V, V _{GS} =10V, R _G =3.3, I _D =4A	---	8	---	ns
T _r	Rise Time		---	14.2	---	
Td(off)	Turn-Off Delay Time		---	24.4	---	
T _f	Fall Time		---	4.6	---	
Ciss	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	1378	---	pF
Coss	Output Capacitance		---	86	---	
Crss	Reverse Transfer Capacitance		---	64	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	4.8	A
ISM	Pulsed Source Current ^{2,5}		---	---	9.6	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation

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P-Channel Electrical Characteristics (T_J =25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-60	-70	---	V
ΔBVDSS/ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.03	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-3A	---	48	58	mΩ
		V _{GS} =-4.5V, I _D =-2A	---	64	80	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.2	-1.6	-2.5	V
ΔVGS(th)	V _{GS(th)} Temperature Coefficient		---	4.56	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =-48V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-48V, V _{GS} =0V, T _J =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	15	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13.5	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-48V, V _{GS} =-4.5V, I _D =-3A	---	9.86	---	nC
Q _{gs}	Gate-Source Charge		---	3.1	---	
Q _{gd}	Gate-Drain Charge		---	2.95	---	
Td(on)	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	28.8	---	ns
T _r	Rise Time		---	19.8	---	
Td(off)	Turn-Off Delay Time		---	60.8	---	
T _f	Fall Time		---	7.2	---	
Ciss	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1447	---	pF
Coss	Output Capacitance		---	97.3	---	
Crss	Reverse Transfer Capacitance		---	70	---	
IS	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-3.7	A
ISM	Pulsed Source Current ^{2,5}		---	---	-7.5	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

60V N+P-Channel Enhancement Mode MOSFET

N-Channel Typical Characteristics

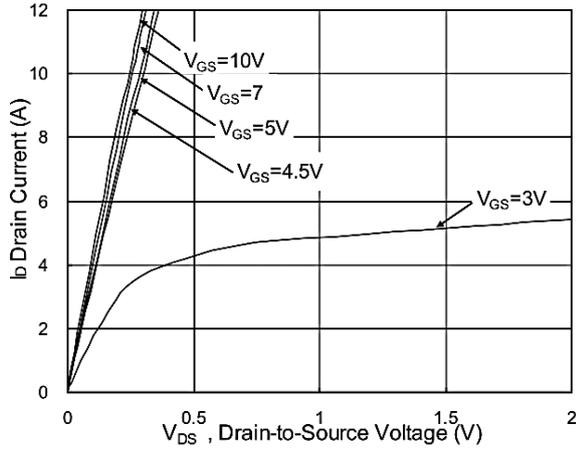


Fig.1 Typical Output Characteristics

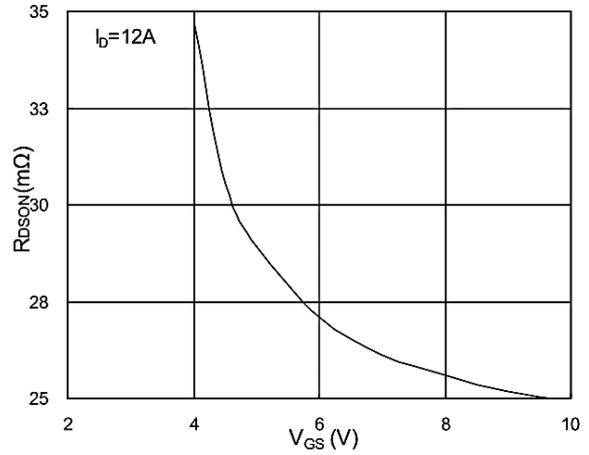


Fig.2 On-Resistance v.s Gate-Source

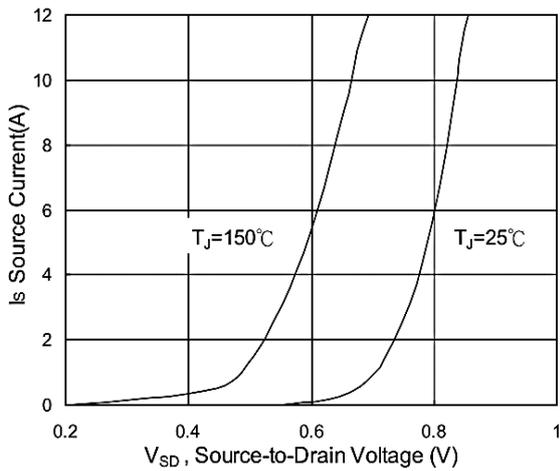


Fig.3 Forward Characteristics of Reverse

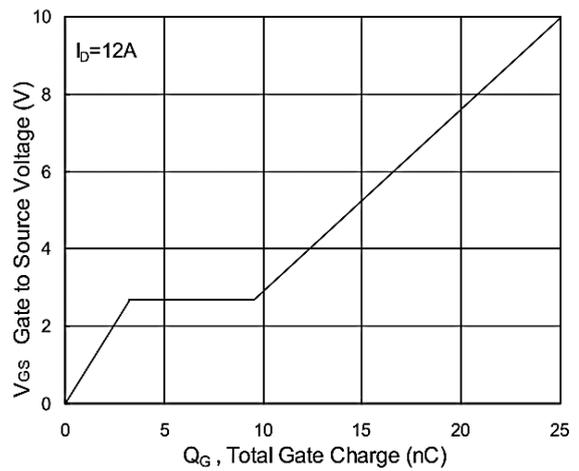


Fig.4 Gate-Charge Characteristics

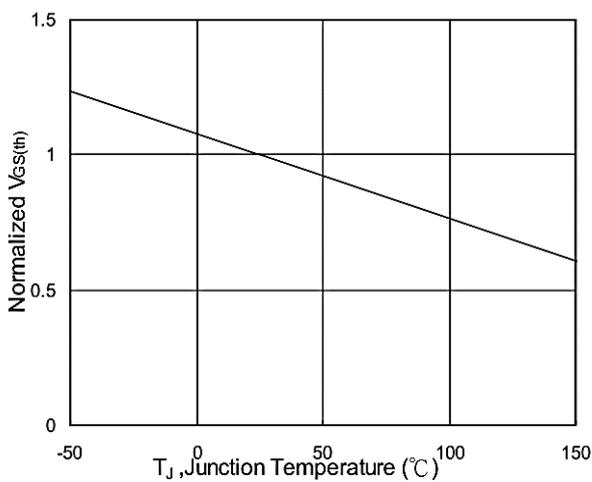


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

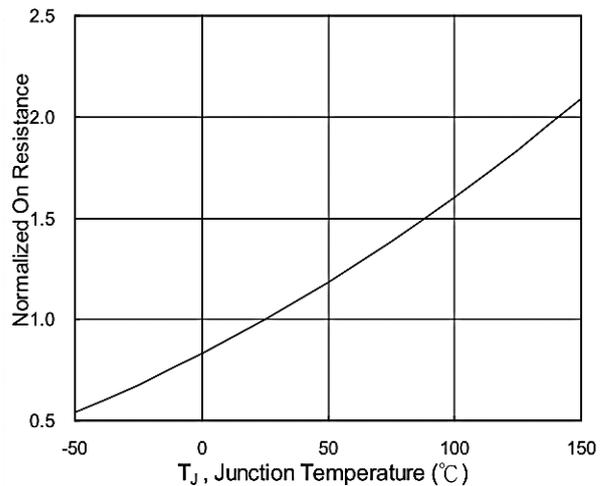


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

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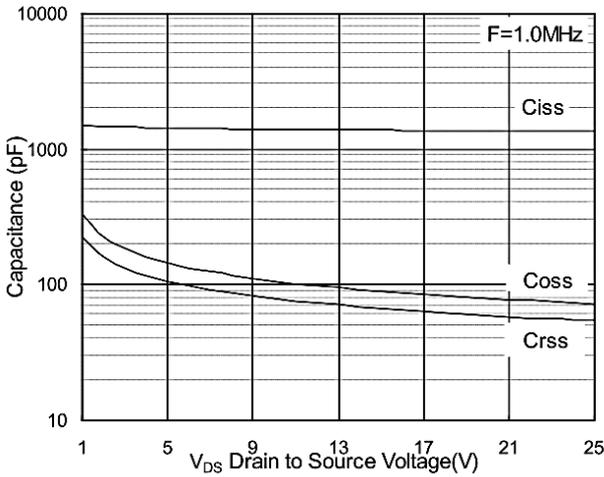


Fig.7 Capacitance

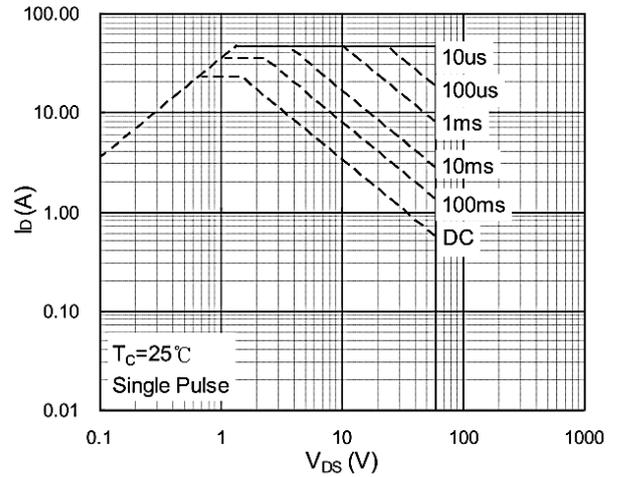


Fig.8 Safe Operating Area

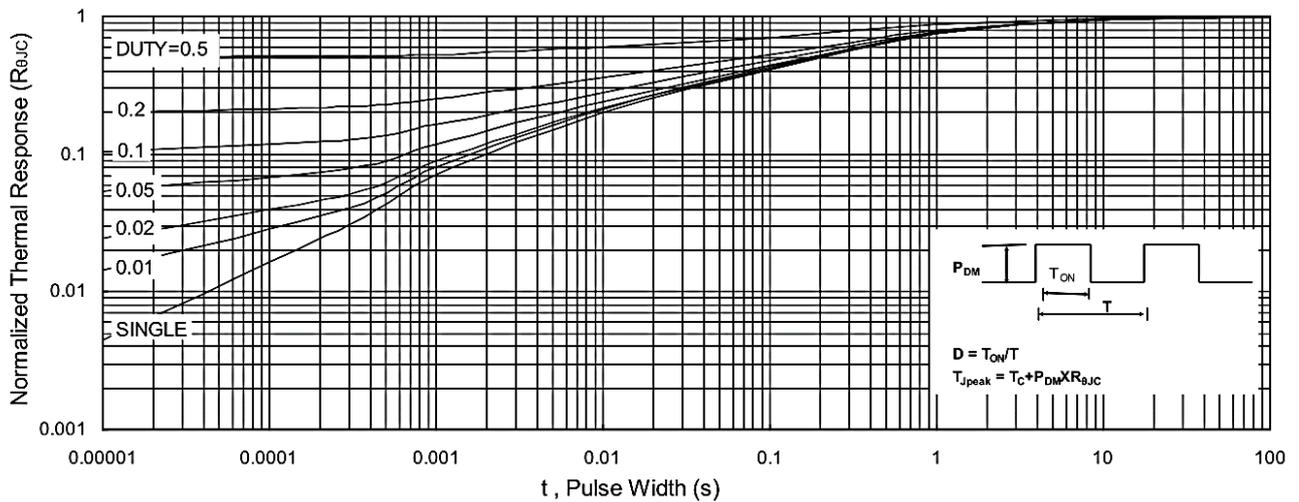


Fig.9 Normalized Maximum Transient Thermal Impedance

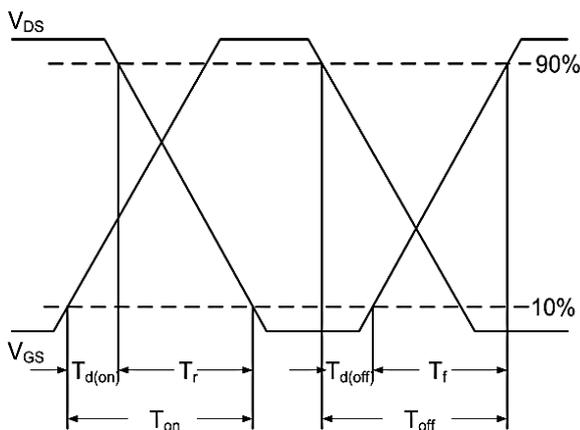


Fig.10 Switching Time Waveform

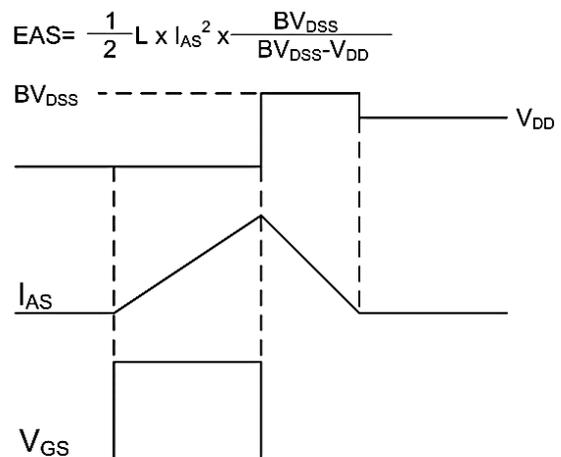


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

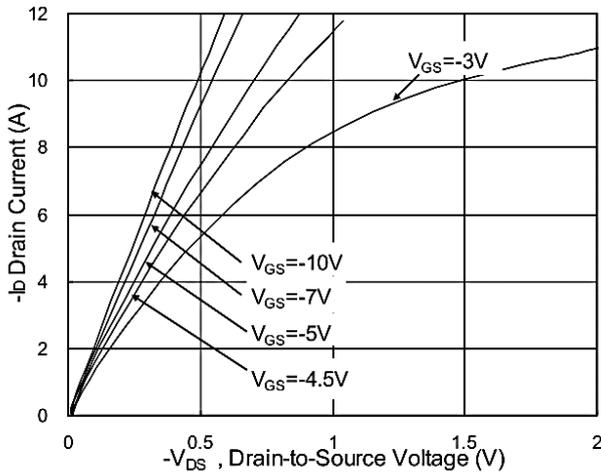


Fig.1 Typical Output Characteristics

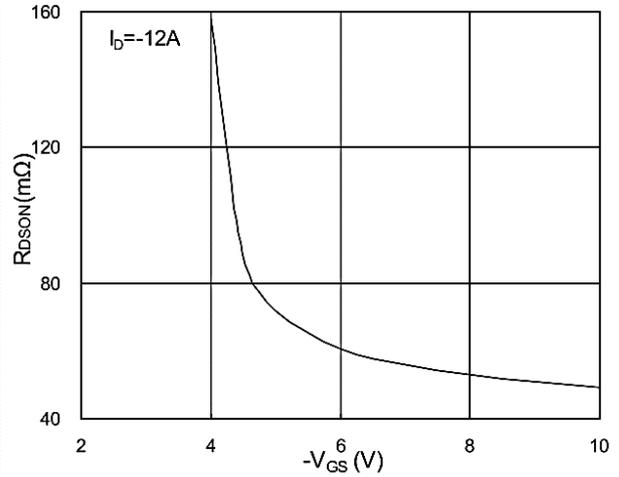


Fig.2 On-Resistance v.s Gate-Source

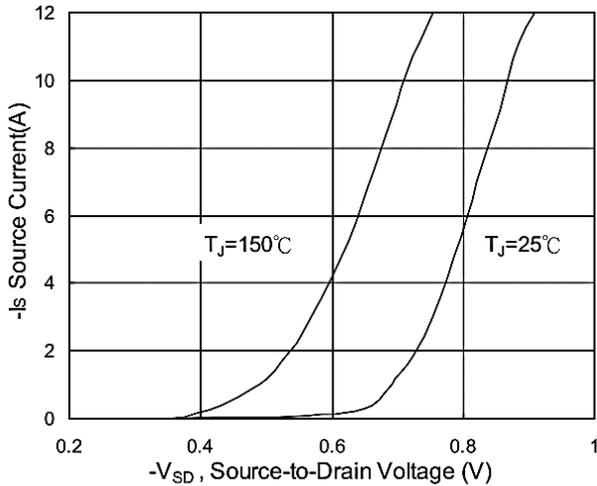


Fig.3 Forward Characteristics of Reverse

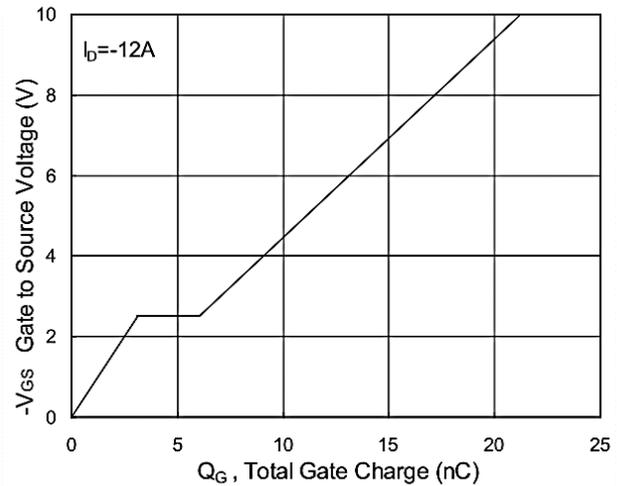


Fig.4 Gate-Charge Characteristics

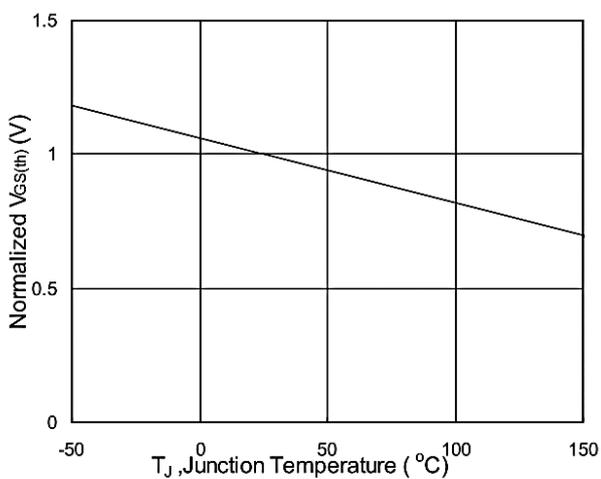


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

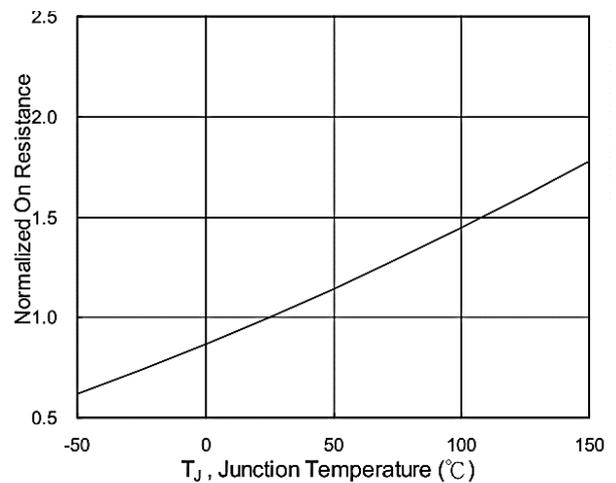


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

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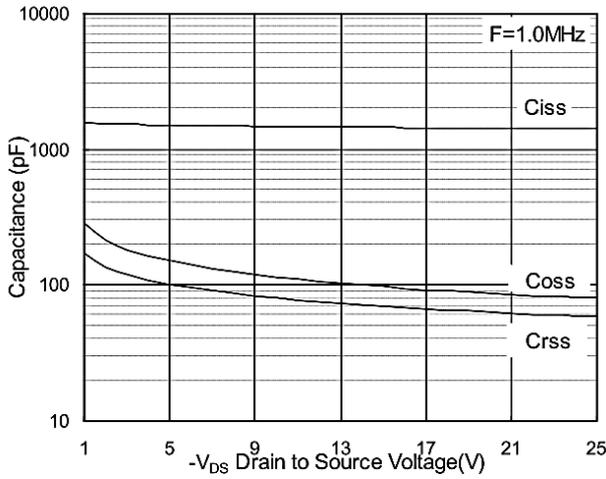


Fig.7 Capacitance

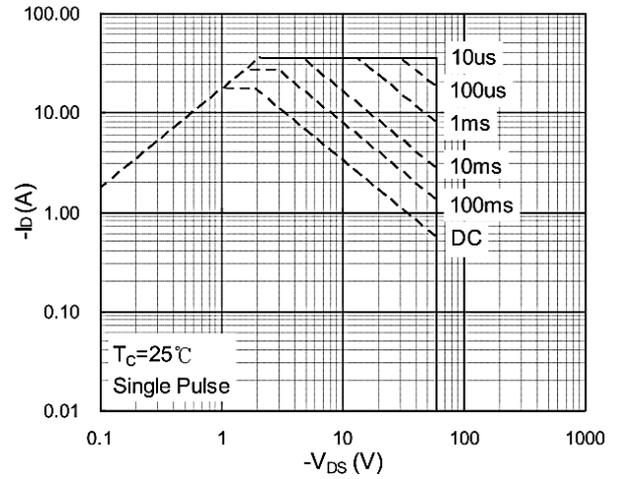


Fig.8 Safe Operating Area

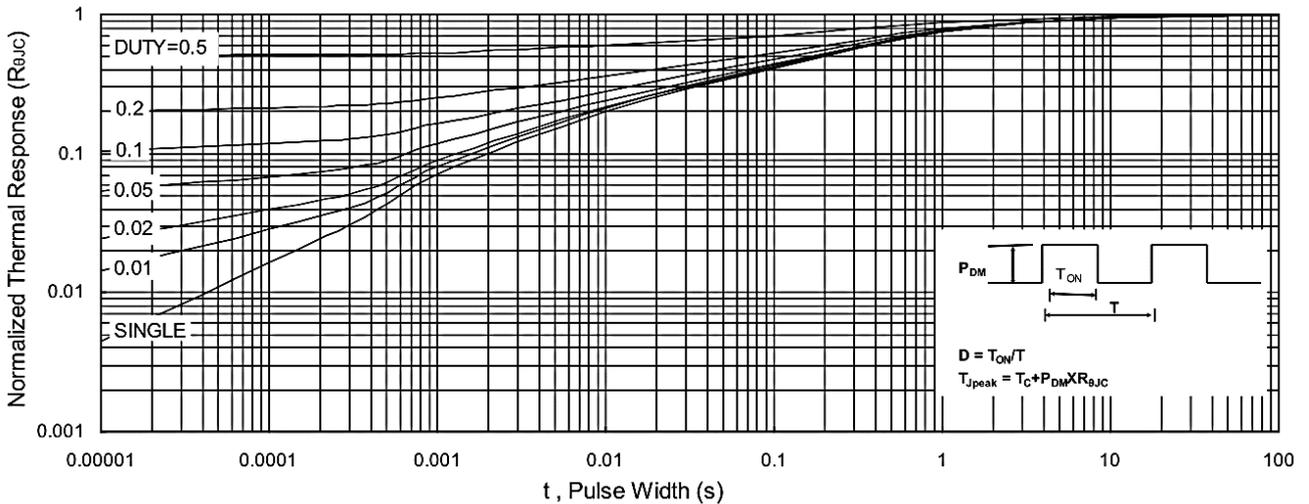


Fig.9 Normalized Maximum Transient Thermal Impedance

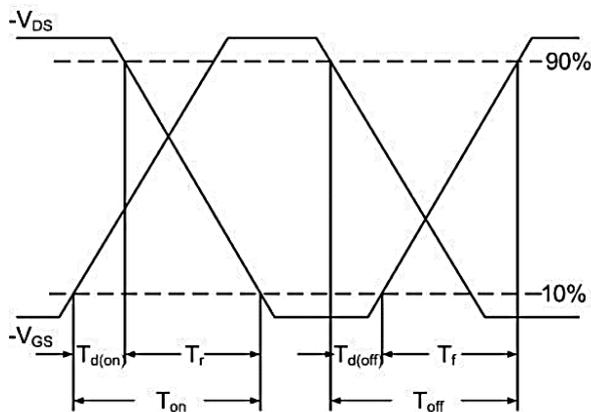


Fig.10 Switching Time Waveform

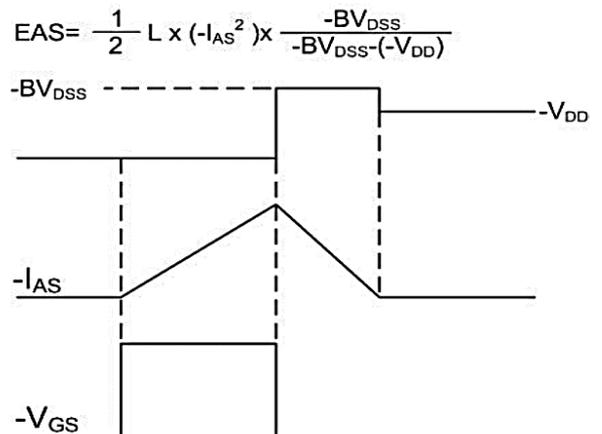
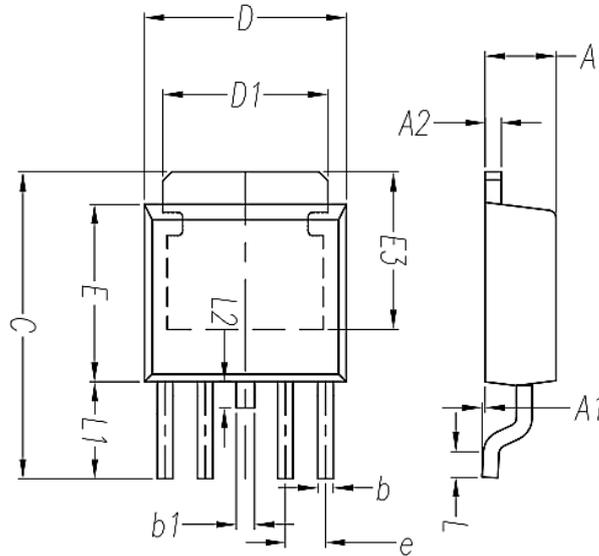


Fig.11 Unclamped Inductive Waveform

Package Mechanical Data-TO-252-4L-Duble-DX



Symbol	Common		
	mm		
	Min	Nom	Max
D	6.30	6.55	6.80
D1	4.80	5.35	5.90
C	9.70	10.00	10.30
E	5.90	6.10	6.30
E3	4.50	5.15	5.80
L	0.90	1.35	1.80
L1	2.60	2.85	3.05
L2	0.50	0.85	1.20
b	0.30	0.50	0.70
b1	0.40	0.60	0.80
A	2.10	2.30	2.50
A2	0.40	0.53	0.65
A1	0.00	0.10	0.20
e	1.17	1.27	1.37

60V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2023/3/31	Initial release

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