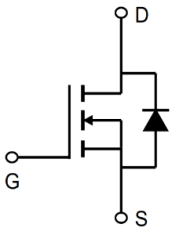
AP2N20MI

200V N-Channel Enhancement Mode MOSFET

Description

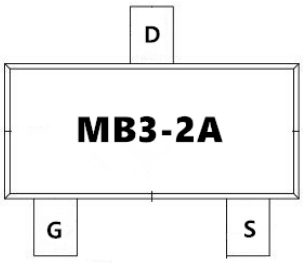
The AP2N20MI is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system



General Features

VDS =200V,ID =2A

RDS(ON) <1800mΩ@ VGS=10V



Application

LED dimming

Emergency lamp

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2N20MI	SOT23-3L	MB3-2A	3000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Limit	Unit
VDS	Drain-Source Voltage	200	V
VGS	Gate-Source Voltage	±20	V
I_D	Drain Current-Continuous	2	A
IDM	Drain Current-Pulsed (Note 1)	10	A
P_D	Maximum Power Dissipation	3	W
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	℃
RθJA	Thermal Resistance,Junction-to-Ambient (Note 2)	41.7	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	200	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=200V,V_{GS}=0V	-	-	1	μA
IGSS	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	-	3.0	V
RDS(ON)	Drain-Source On-State Resistance	V_{GS}=10V, I_D=2A	-	1400	1800	mΩ
gFS	Forward Transconductance	V_{DS}=15V,I_D=2A	-	8	-	S
C_{lss}	Input Capacitance	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	580	-	PF
Coss	Output Capacitance		-	90	-	PF
C_{rss}	Reverse Transfer Capacitance		-	3	-	PF
td(on)	Turn-on Delay Time	V_{DD}=100V, R_L=15Ω V_{GS}=10V,R_G=2.5Ω	-	10	-	nS
t_r	Turn-on Rise Time		-	12	-	nS
td(off)	Turn-Off Delay Time		-	15	-	nS
t_f	Turn-Off Fall Time		-	15	-	nS
Q_g	Total Gate Charge	V_{DS}=100V,I_D=2A, V_{GS}=10V	-	12		nC
Q_{gs}	Gate-Source Charge		-	2.5	-	nC
Q_{gd}	Gate-Drain Charge		-	3.8	-	nC
VSD	Diode Forward Voltage (Note 3)	V_{GS}=0V,I_S=2A	-	-	1.2	V
I_S	Diode Forward Current (Note 2)		-	-	2	A

Notes:

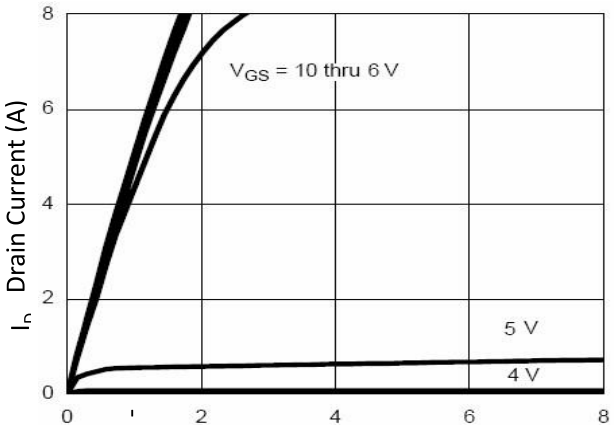
1、Repetitive Rating: Pulse width limited by maximum junction temperature.

2、Surface Mounted on FR4 Board, t ≤ 10 sec.

3、Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

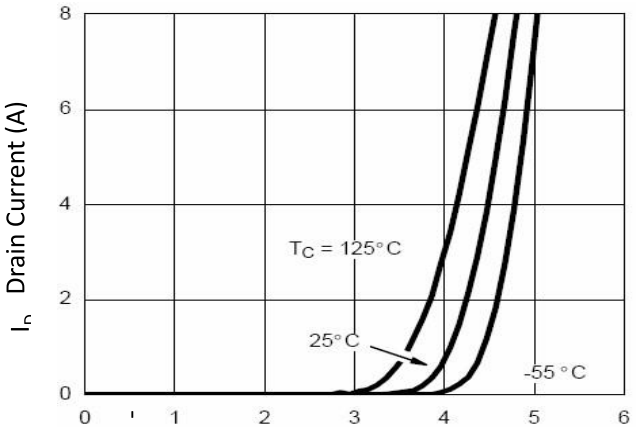
4、Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics (Curves)



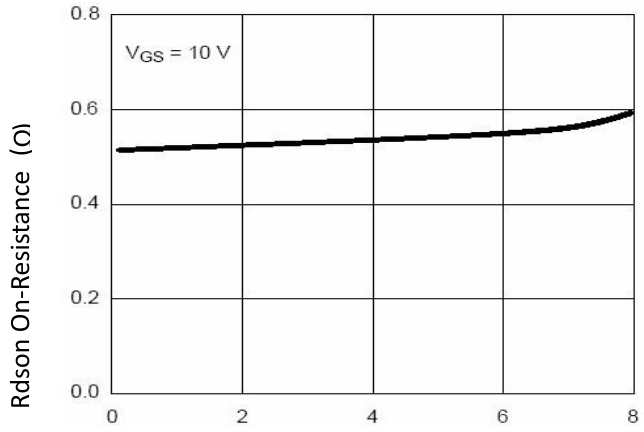
Vds Drain-Source Voltage (V)

Figure 1 Output Characteristics



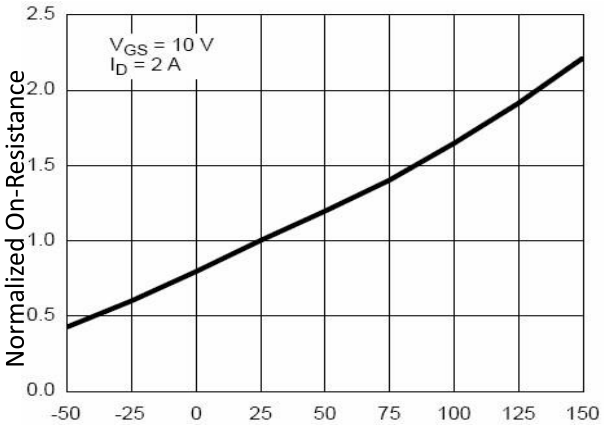
Vgs Gate-Source Voltage (V)

Figure 2 Transfer Characteristics



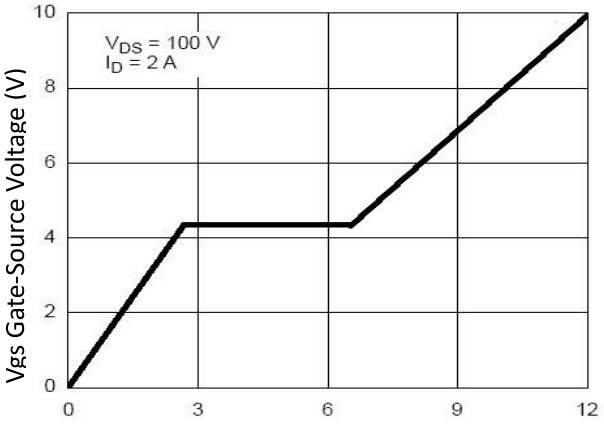
ID- Drain Current (A)

Figure 3 Rdson- Drain Current



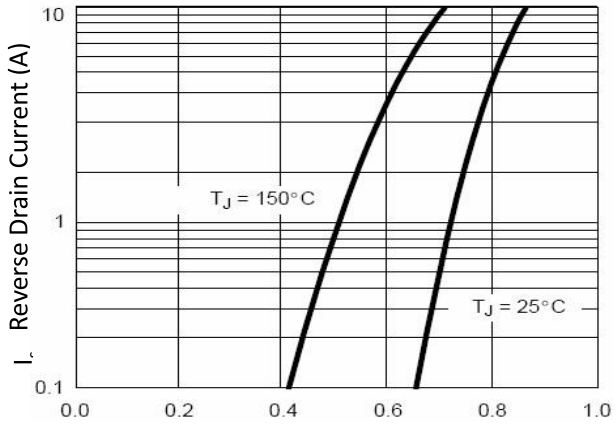
TJ-Junction Temperature (℃)

Figure 4 Rdson-JunctionTemperature



Qg Gate Charge (nC)

Figure 5 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

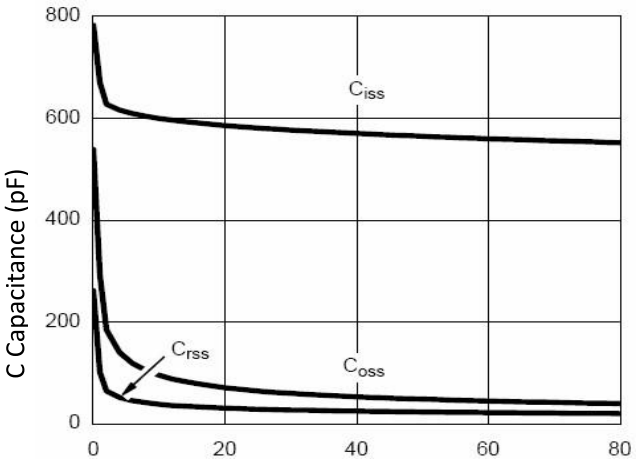


Figure 7 Capacitance vs Vds

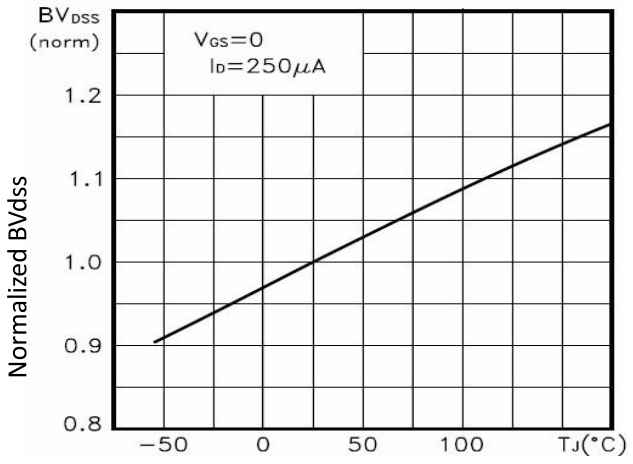


Figure 9 BV_{DSS} vs Junction Temperature

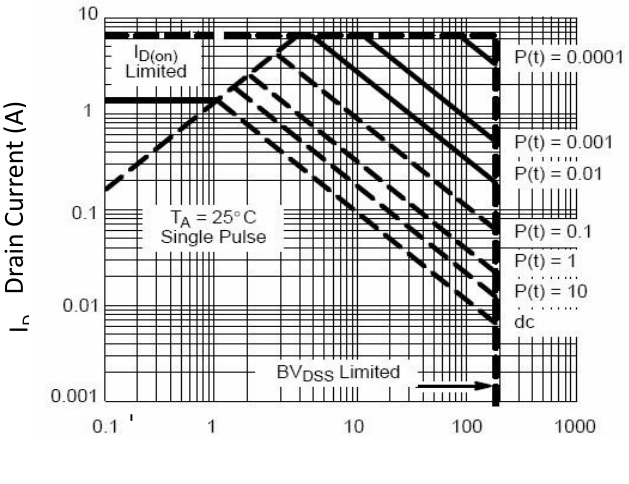


Figure 8 Safe Operation Area

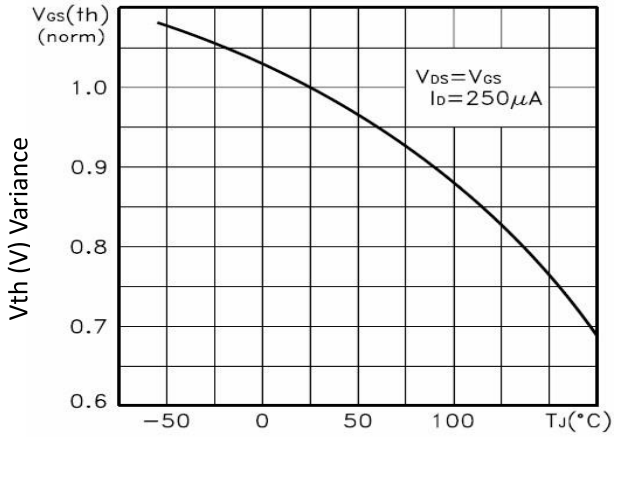


Figure 10 $V_{GS(th)}$ vs Junction Temperature

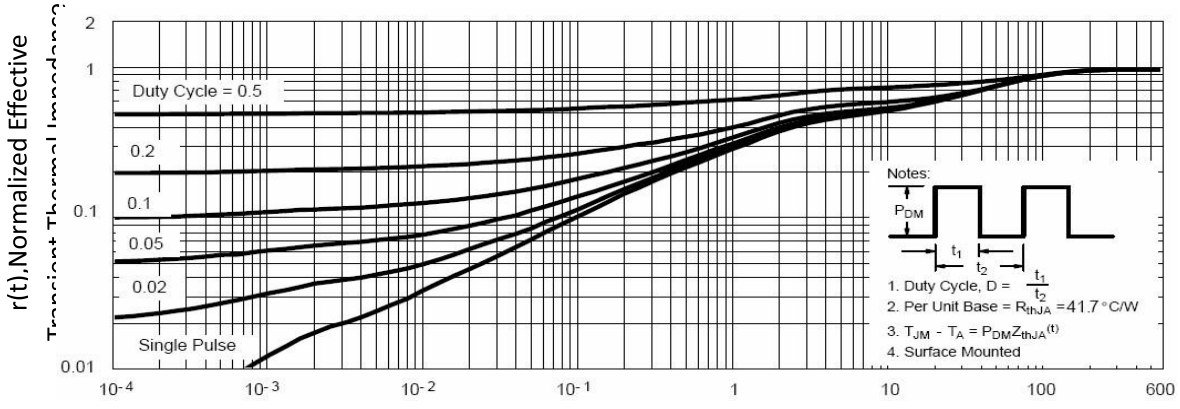
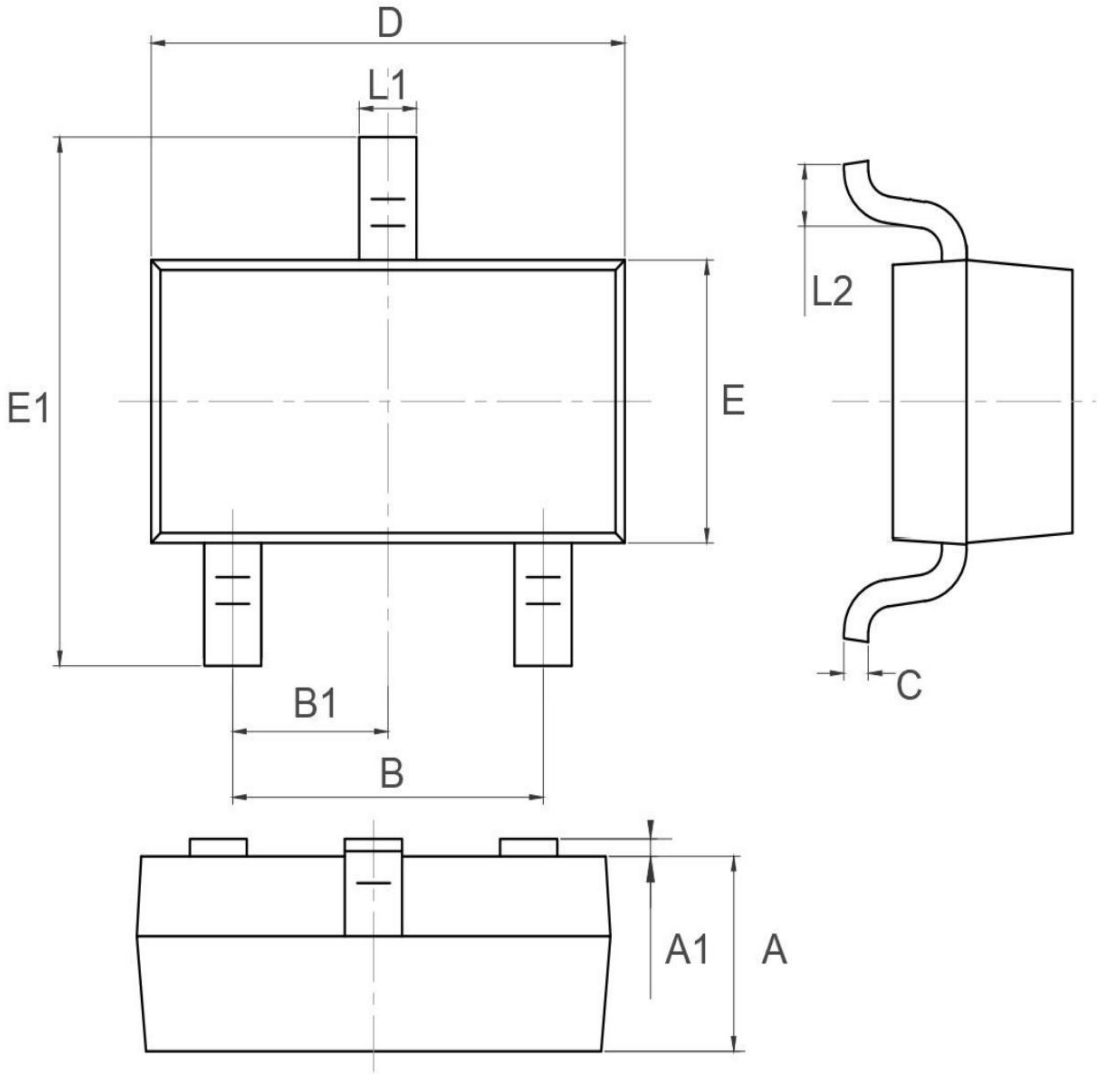


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data：SOT23-3L



Symbol	Dim in mm		
	min.	typ.	max.
A	1	1.1	1.2
A1	0	0.05	0.1
B	1.8	1.9	2
B1		0.95TYP	
C	0.1	0.15	0.2
D	2.82	2.92	3.02
E	1.5	1.6	1.7
E1	2.65	2.8	2.95
L1	0.3	0.4	0.5
L2	0.3	0.45	0.6

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200V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve3.2	2018/1/31	Initial release
Rve3.3	2019/12/01	Reduce RDS
Rve3.4	2020/4/01	Reduce VTH
Rve3.5	2025/6/04	Update LOGO And Corrected Manual POD