AP25G04GD

40V N+P-Channel Enhancement Mode MOSFET

Description

The AP25G04GD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = 40V I_D =28A

$R_{DS(ON)}$ < 18mΩ @ V_{GS}=10V （**Type：14mΩ**）

V_{DS} = -40V I_D =-25A

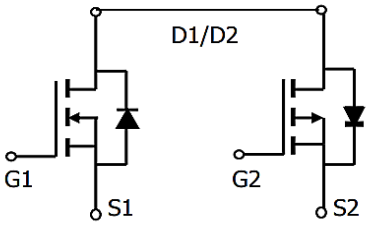
$R_{DS(ON)}$ < 36mΩ @ V_{GS}=-10V （**Type：31mΩ**）

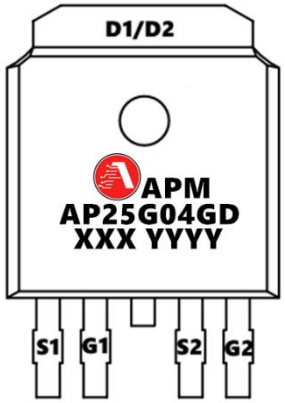
Application

Wireless charging

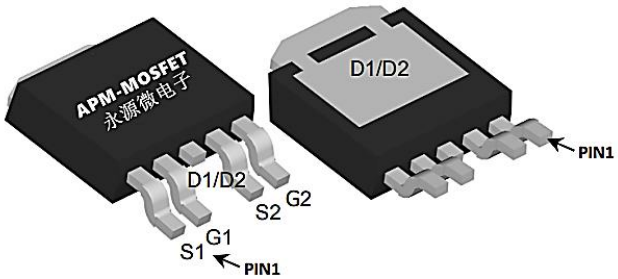
Boost driver

Brushless motor





Top View Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP25G04GD	TO-252-4L	AP25G04GD XXX YYYY	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
VDS	Drain-Source Voltage	40	-40	V
VGS	Gate-Source Voltage	±20	±20	V
I_D@T_A=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	28	25	A
I_D@T_A=70℃	Continuous Drain Current, V_{GS} @ 10V[1]	18	-16	A
IDM	Pulsed Drain Current[2]	65	-60	A
EAS	Single Pulse Avalanche Energy[3]	160	155	mJ
P_D@T_A=25℃	Total Power Dissipation[4]	26		W
TSTG	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃
R_{θ}JA	Thermal Resistance Junction-Ambient [1]	62.5		℃/W
R_{θ}JC	Thermal Resistance Junction-Case[1]	5		℃/W

N-Channel Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.5	2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	V_{GS}=10V, I_D=8A	-	14	18	mΩ
		V_{GS}=4.5V, I_D=5A	-	16	25	mΩ
Ciss	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1.0MHz	-	1342	-	pF
Coss	Output Capacitance		-	84	-	pF
Crss	Reverse Transfer Capacitance		-	72	-	pF
Q_g	Total Gate Charge	V_{DS}=20V, I_D=8A, V_{GS}=10V	-	26	-	nC
Qgs	Gate-Source Charge		-	6	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	5	-	nC
td(on)	Turn-on Delay Time	V_{DD}= 20V, V_{GS}=10V,R_{REN} =3Ω	-	7	-	ns
tr	Turn-on Rise Time		-	11	-	ns
td(off)	Turn-off Delay Time		-	26	-	ns
t_f	Turn-off Fall Time		-	5	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	28	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	62	A
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S= 20A	-	-	1.2	V

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,IAS=10A

4、The power dissipation is limited by 150℃ junction temperature

5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= -250μA	-40	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS}= -40V, V_{GS}=0V	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= -250μA	-1.0	-1.6	-2.5	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS}= -10V, I_D= -6A	-	31	36	mΩ
		V_{GS}= -4.5V, I_D= -5A	-	40	48	
Ciss	Input Capacitance	V_{DS}= -20V, V_{GS}=0V, f=1.0MHz	-	1080	-	pF
Coss	Output Capacitance		-	87	-	pF
Crss	Reverse Transfer Capacitance		-	77	-	pF
Q_g	Total Gate Charge	V_{DS}= -20V, I_D= -5A, V_{GS}= -10V	-	17	-	nC
Qgs	Gate-Source Charge		-	4.2	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	3.7	-	nC
td(on)	Turn-on Delay Time	V_{DD}= -20V, I_D= -5A, V_{GS}= -10V, R_{GEN}=2.5Ω	-	5.9	-	ns
tr	Turn-on Rise Time		-	7.1	-	ns
td(off)	Turn-off Delay Time		-	25	-	ns
t_f	Turn-off Fall Time		-	8.2	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-21	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-60	A
trr	Reverse Recovery Time	T_J=25℃, I_F=10A,dI/dt=100A/μs	-	10	-	ns
Qrr	Reverse Recovery Charge		-	6	-	nC
VSD	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S= -10A	-	-0.8	-1.2	V

Note :

1、The data tested by surface mo unted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The EAS data shows Max. rating . The test condition is V^{DD}=-25V,V^{GS}=-10V,L=0.1mH,IAS=-10A

4、The power dissipation is limited by 150℃ junction temperature

5 、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

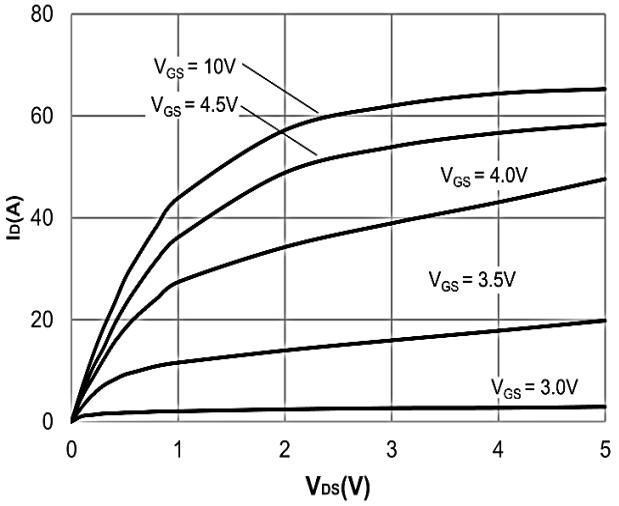


Figure1: Output Characteristics

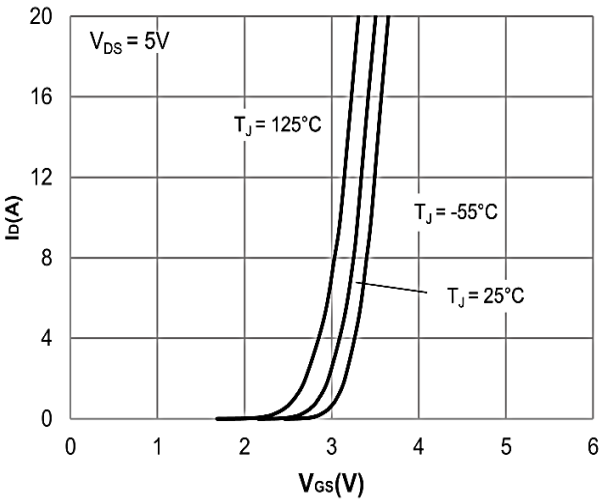


Figure 2: Typical Transfer Characteristics

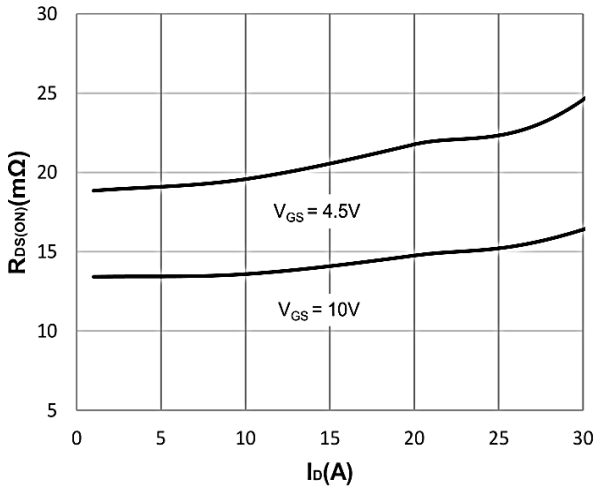


Figure 3:On-resistance vs. Drain Current

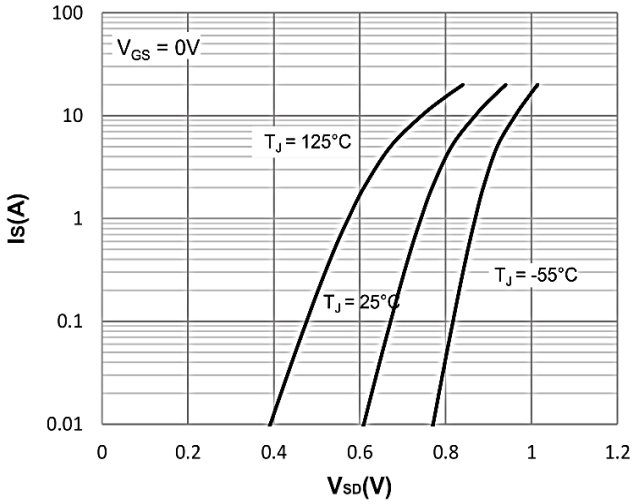


Figure 4: Body Diode Characteristics

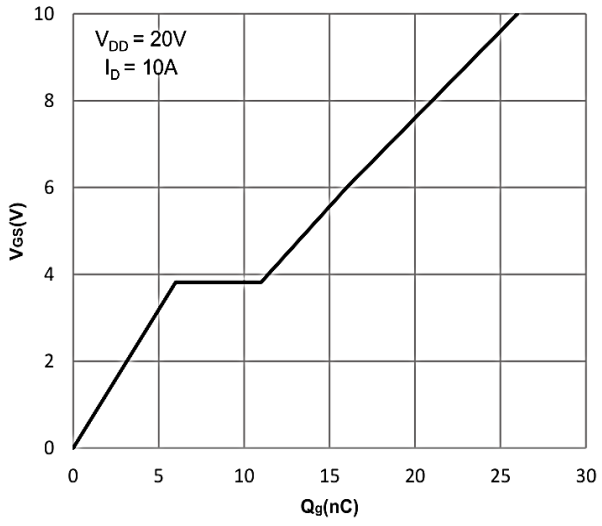


Figure 5: Gate Charge Characteristics

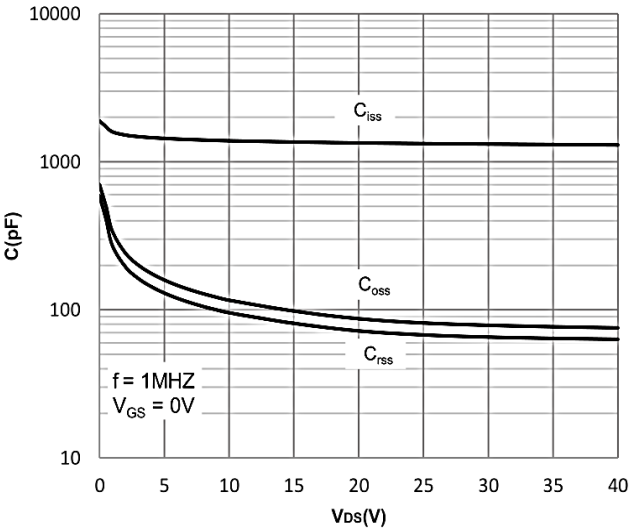


Figure 6: Capacitance Characteristics

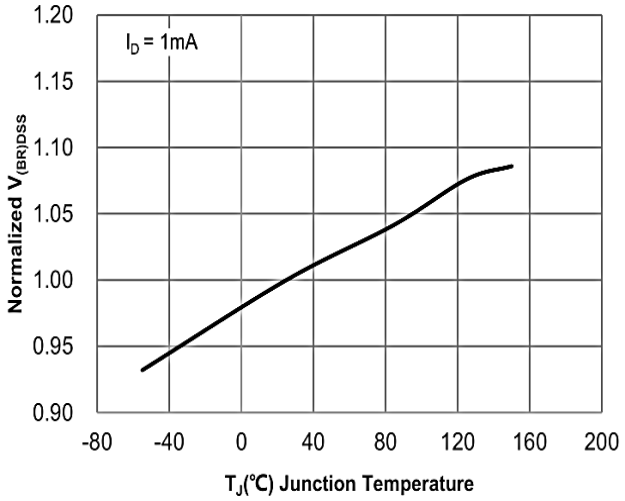


Figure 7: Normalized Breakdown Voltage vs Junction Temperature

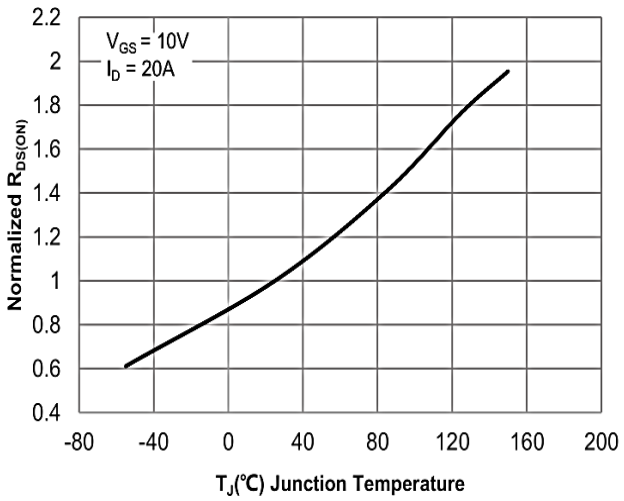


Figure 8: Normalized on Resistance vs. Junction Temperature

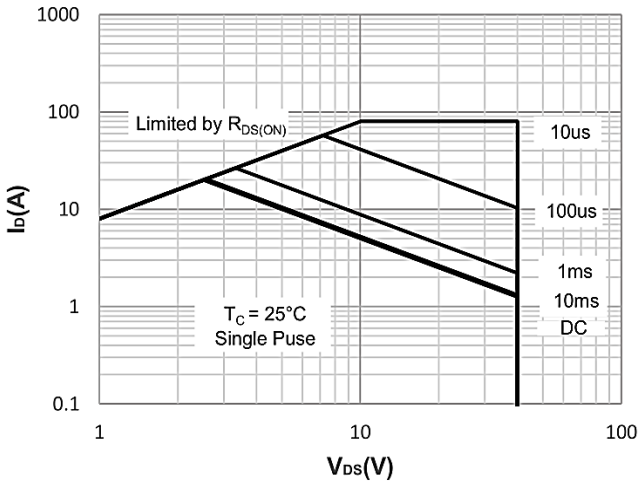


Figure 9: Maximum Safe Operating Area

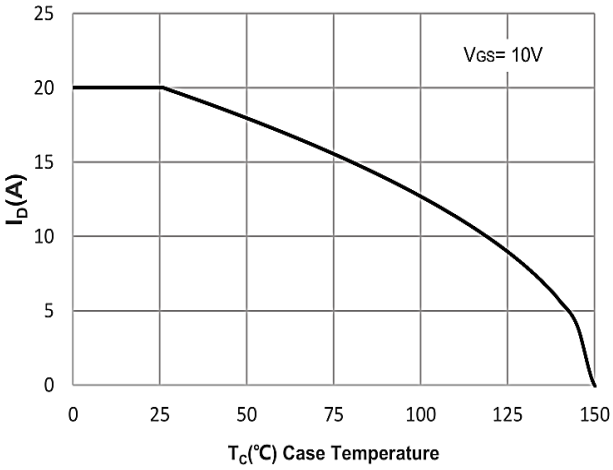


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

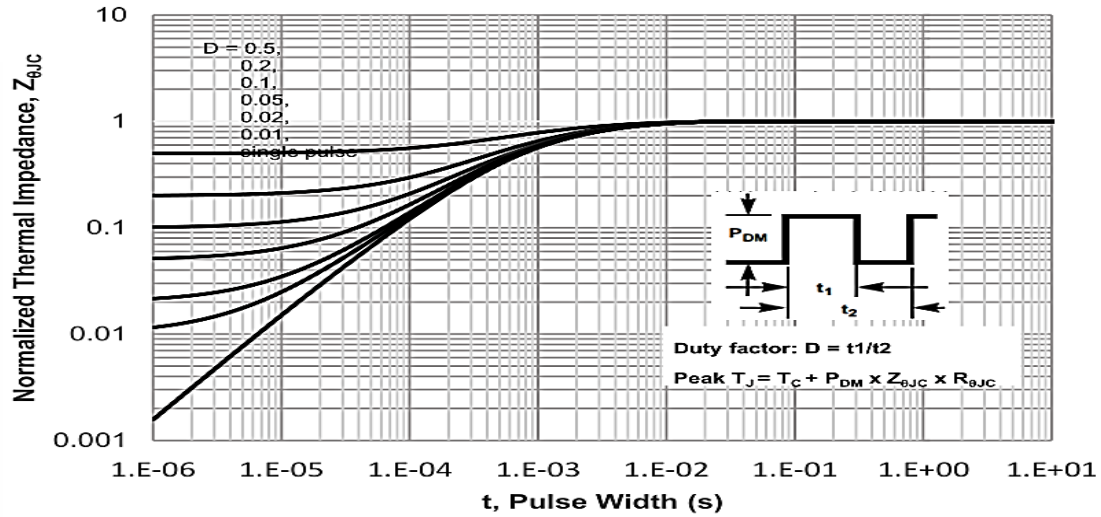


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambien

P-Typical Characteristics

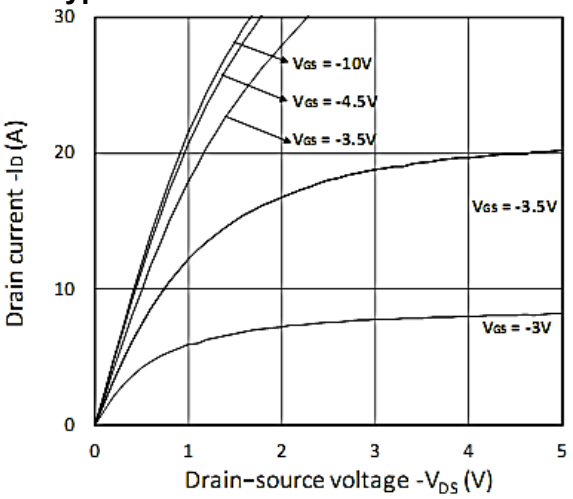


Figure 1. Output Characteristics

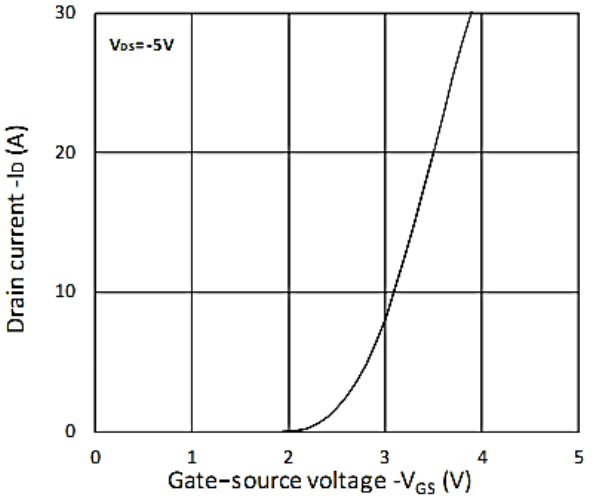


Figure 2. Transfer Characteristics

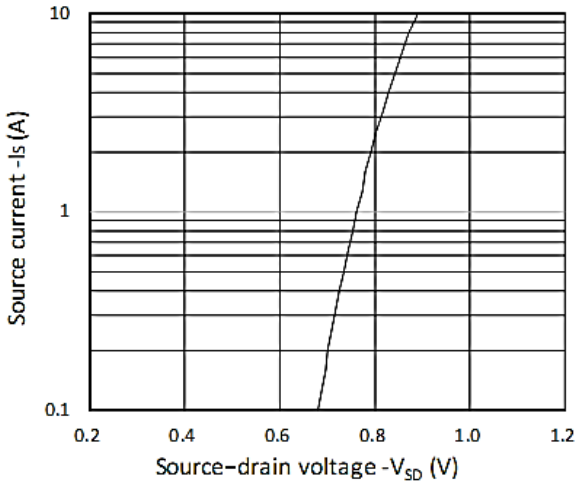


Figure 3. Forward Characteristics of Reverse

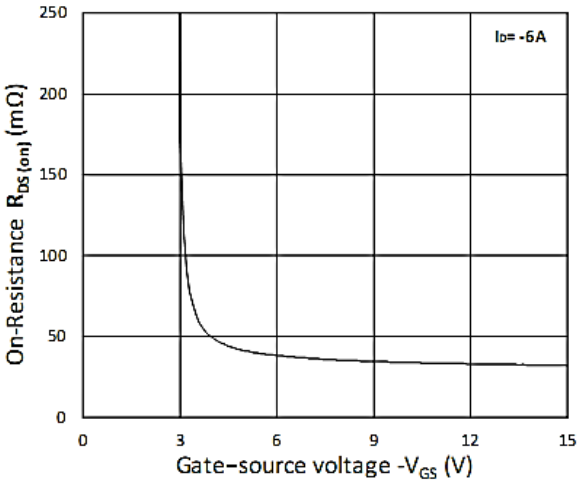


Figure 4. R DS(ON) vs. VGS

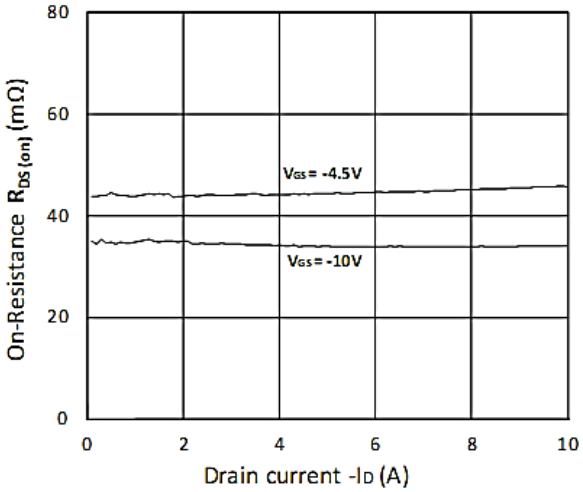


Figure 5. RDS(ON) vs. ID

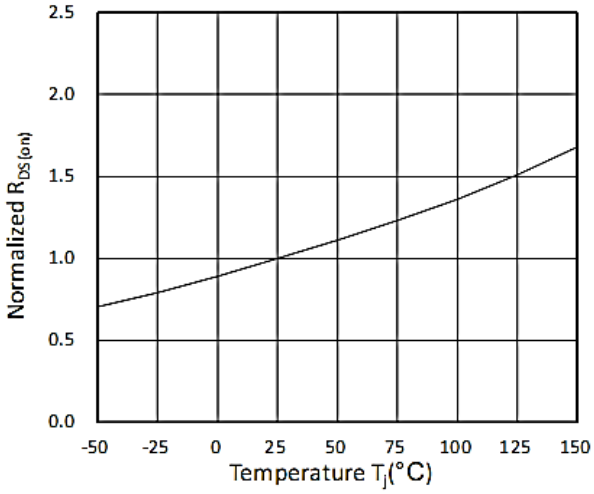


Figure 6. Normalized RDS(on) vs. Temperature

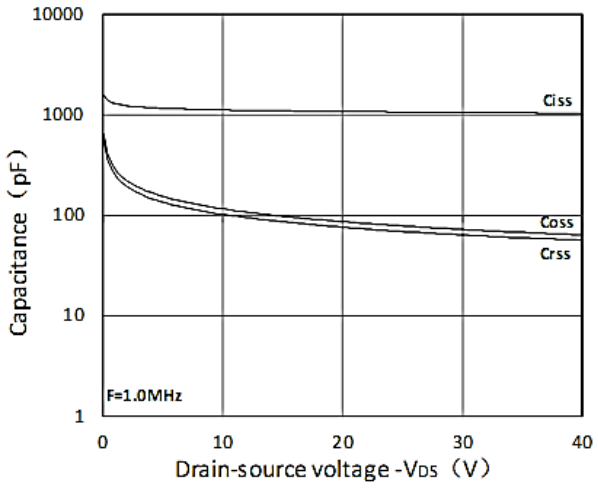


Figure 7. Capacitance Characteristics

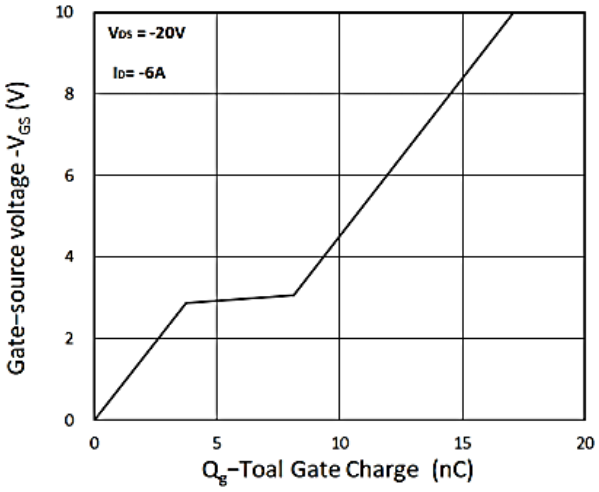


Figure 8. Gate Charge Characteristics

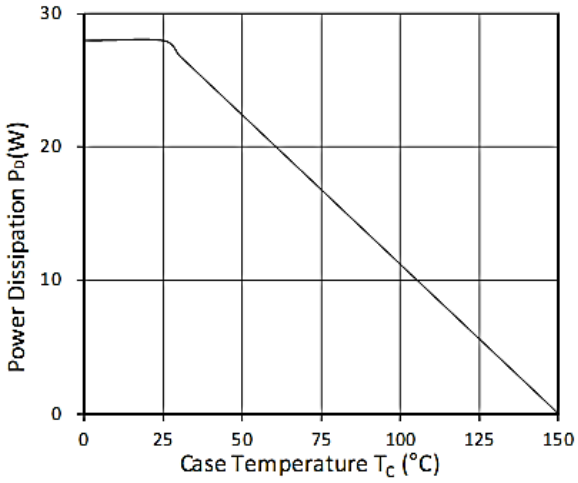


Figure 9. Power Dissipation

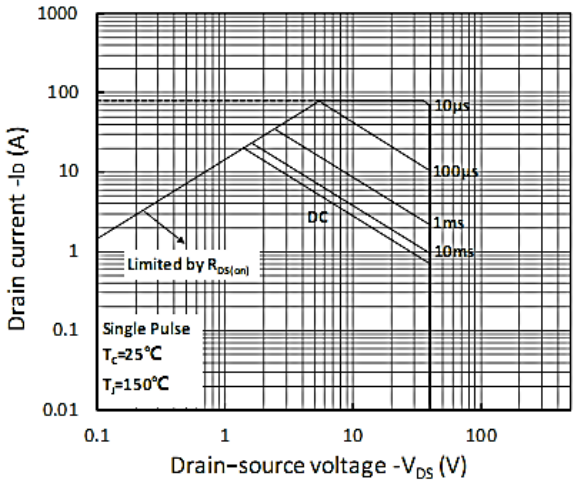


Figure10. Safe Operating Area

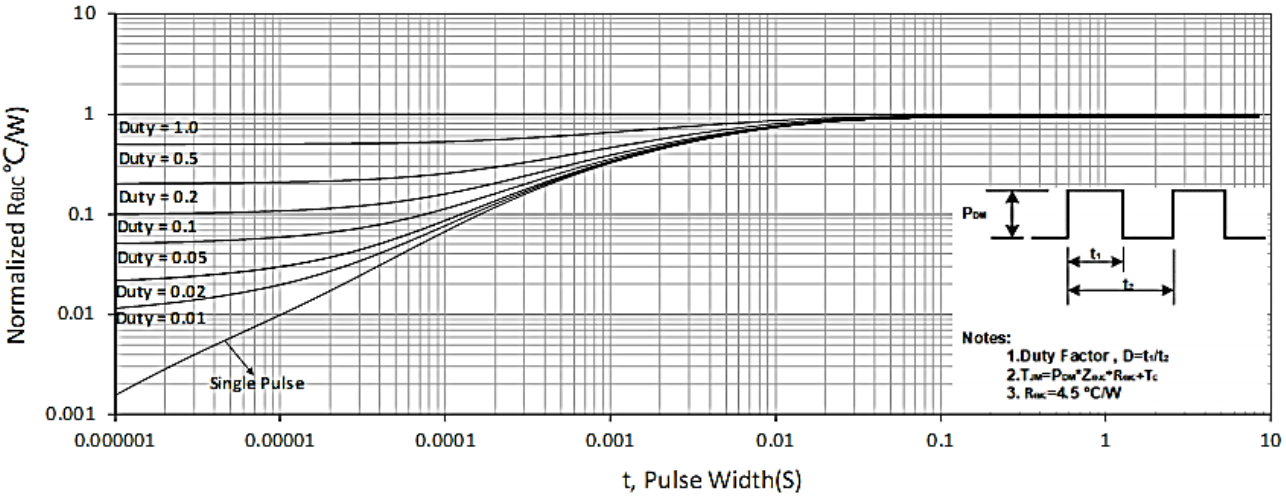
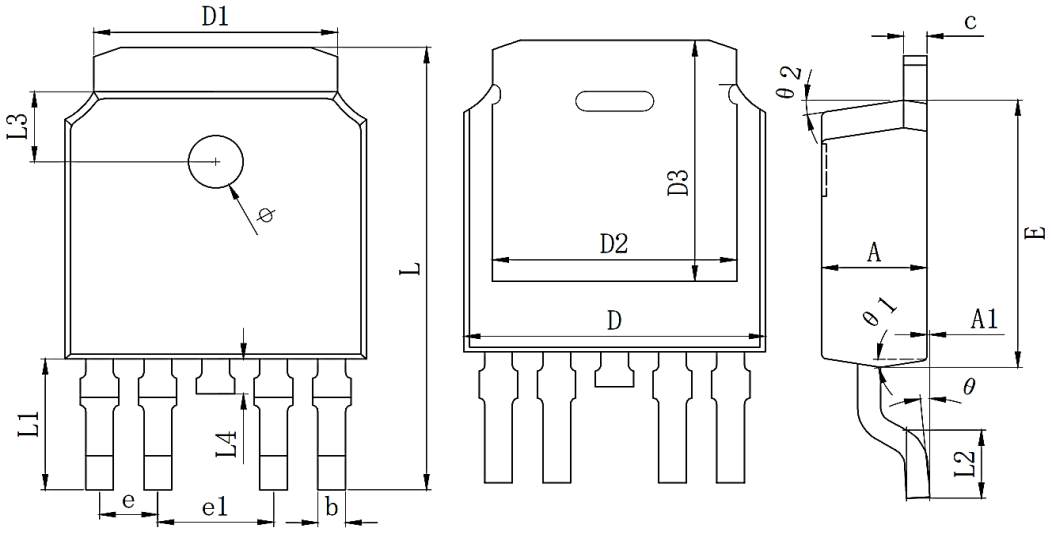


Figure 9 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data:TO-252-4L



Symbol	Dim in mm		
	Min	Typ	max
A	2.1	2.3	2.5
A1	0	0.064	0.128
b	0.5	0.6	0.7
c	0.45	0.52	0.6
D	6.4	6.6	6.8
D1	5.33REF		
D2	5.06REF		
D3	5.25REF		
E	5.9	6.1	6.3
e	1.27TYP		
e1	2.54TYP		
L	9.8	10.1	10.4
L1	2.888REF		
L2	1.4	1.5	1.7
L3	1.65REF		
L4	0.6	0.8	1
ϕ	1.1	1.2	1.3
θ	0°		10°
θ1	5°		10°
θ2	5°		10°

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Edition	Date	Change
REV1.0	2018/1/31	Initial release
REV1.1	2025/5/19	Reduce RDS