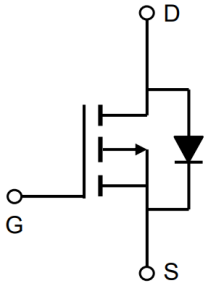
AP2311AI

-18V P-Channel Enhancement Mode MOSFET

Description

The AP2311AI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

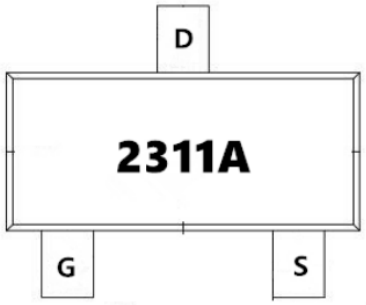


General Features

V_{DS} = -18V I_D =-8.1A

RDS(ON) < 24mΩ @ VGS=10V **(Type：18mΩ)**

RDS(ON) < 26mΩ @ VGS=10V **(Type：20mΩ)**



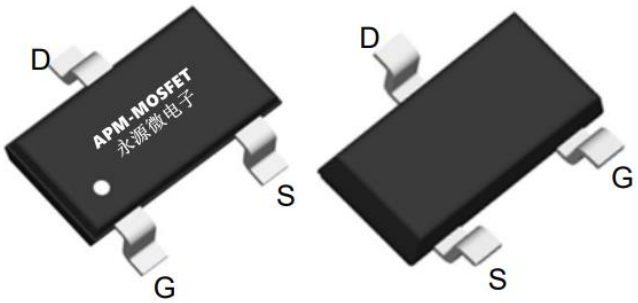
Top View Bottom View

Application

Battery protection

Load switch

Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP2311AI	SOT23L	2311A	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDSS	Drain-Source Voltage	-18	V
VGSS	Gate-Source Voltage	±12	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	-8.1	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	-5.6	A
IDM	Pulsed Drain Current note1	-48	A
P_D@T_C=25℃	Power Dissipation	1.6	W
RθJA	Thermal Resistance, Junction to Ambient	125	℃/W
TJ, TSTG	Operating and Storage Temperature Range	-55 to +150	℃

-18V P-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	VGS=0V, ID=-250μA	-18	-20	-	V
IDSS	Zero Gate Voltage Drain Current	VDS =-12V, VGS = 0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	VDS =0V, VGS = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=-250μA	-0.5	-0.65	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	VGS=-4.5V, ID=-6.0A	-	18	24	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	VGS=-4.5V, ID=-5.2A	-	20	26	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	VGS=-2.5V, ID=-4.2A		28	35	mΩ
Ciss	Input Capacitance	VDS=-6V, VGS=0V f=1.0MHz	-	1100	-	pF
Coss	Output Capacitance		-	390	-	pF
Crss	Reverse Transfer Capacitance		-	300	-	pF
Qg	Total Gate Charge	VDS=-4V, ID=-4.1A, VGS = -4.5V	-	11.5		nC
Qgs	Gate-Source Charge		-	1.5	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	3.2	-	nC
td(on)	Turn-on Delay Time	VDD =-4V, ID=-3.3A, RG=1.0Ω, VGEN=-4.5V, RL=1.2Ω	-	25	-	ns
tr	Turn-on Rise Time		-	45	-	ns
td(off)	Turn-off Delay Time		-	72	-	ns
tf	Turn-off Fall Time		-	60	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-8.1	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-48	A
VSD	Drain to Source Diode Forward Voltage	VGS=0V, IS =-4.1A	-	-	-1.2	V
trr	Reverse Recovery Time	VGS=0V, IS=-4.1A, di/dt=100A/μs	-	20	-	ns
Qrr	Reverse Recovery Charge		-	9	-	nC

Note :

1、The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3、The power dissipation is limited by 150℃ junction temperature

4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

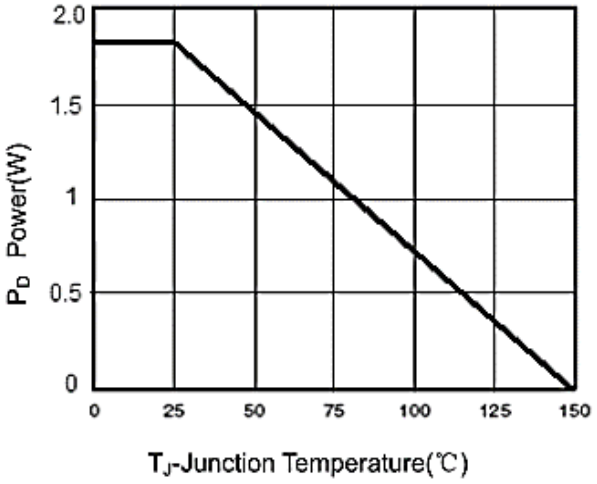


Figure 1 Power Dissipation

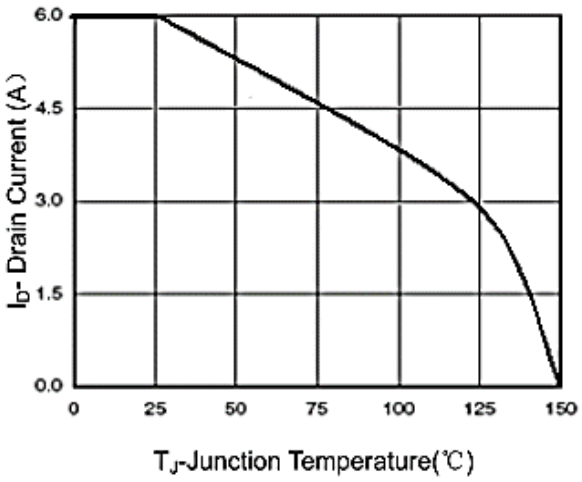


Figure 2 Drain Current

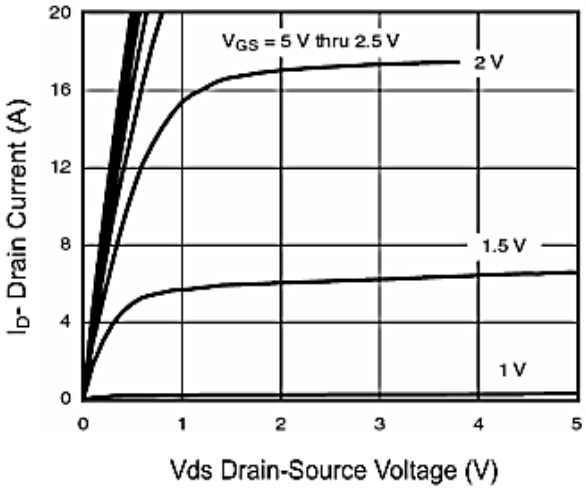


Figure 3 Output Characteristics

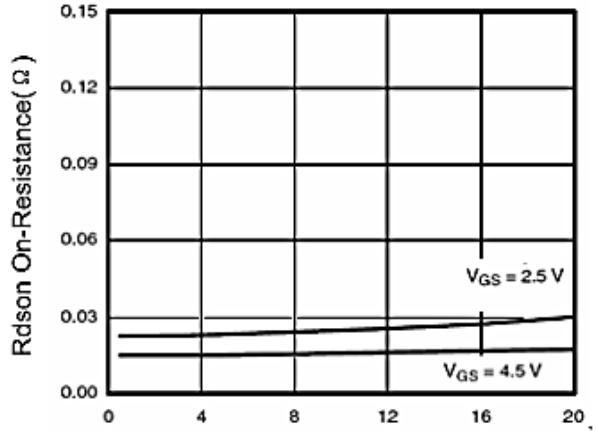


Figure 4 Drain-Source On-Resistance

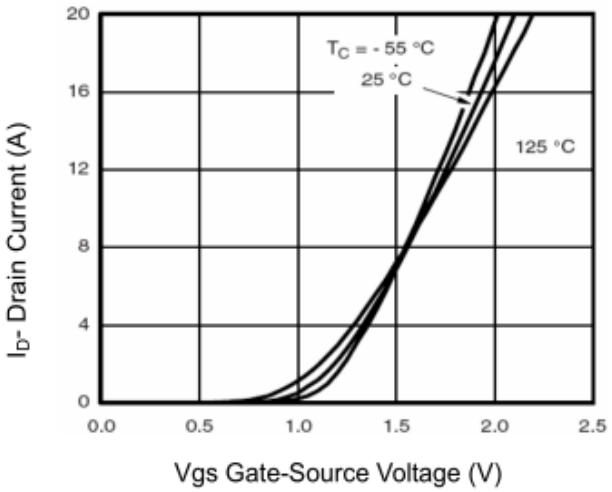


Figure 5 Transfer Characteristics

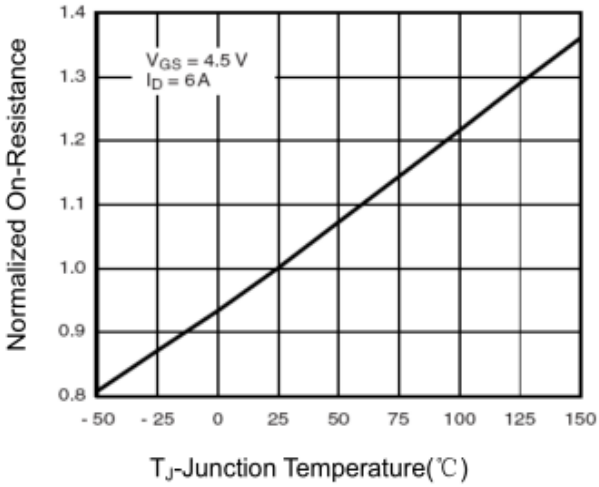


Figure 6 Drain-Source On-Resistance

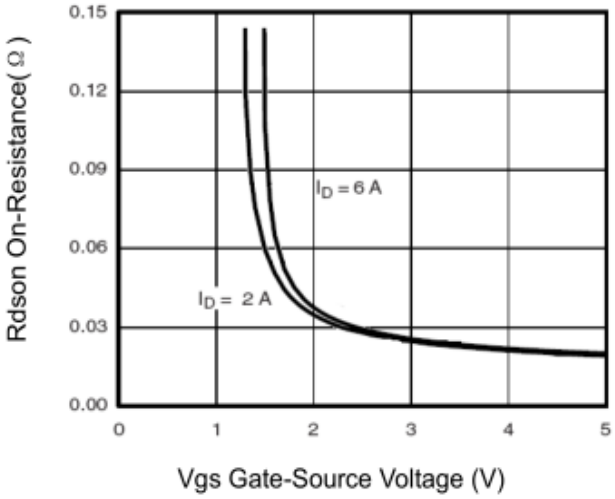


Figure 7 Rdson vs Vgs

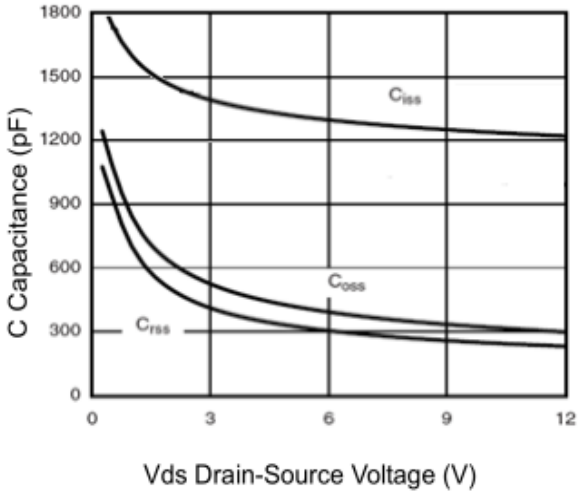


Figure 8 Capacitance vs Vds

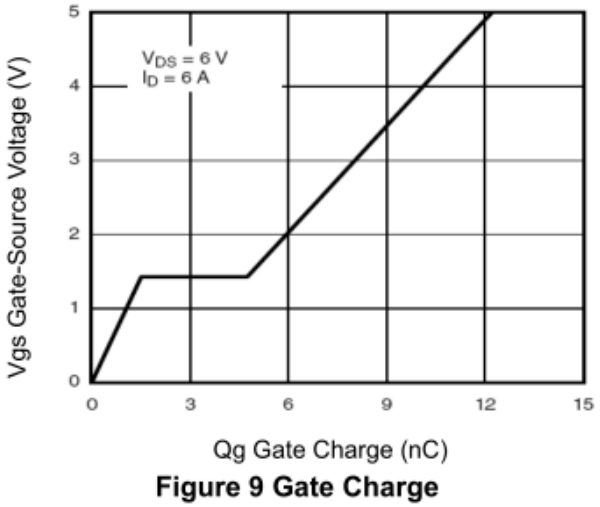


Figure 9 Gate Charge

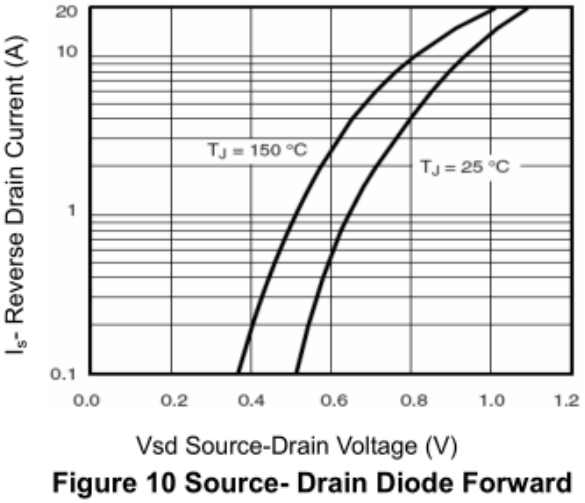


Figure 10 Source- Drain Diode Forward

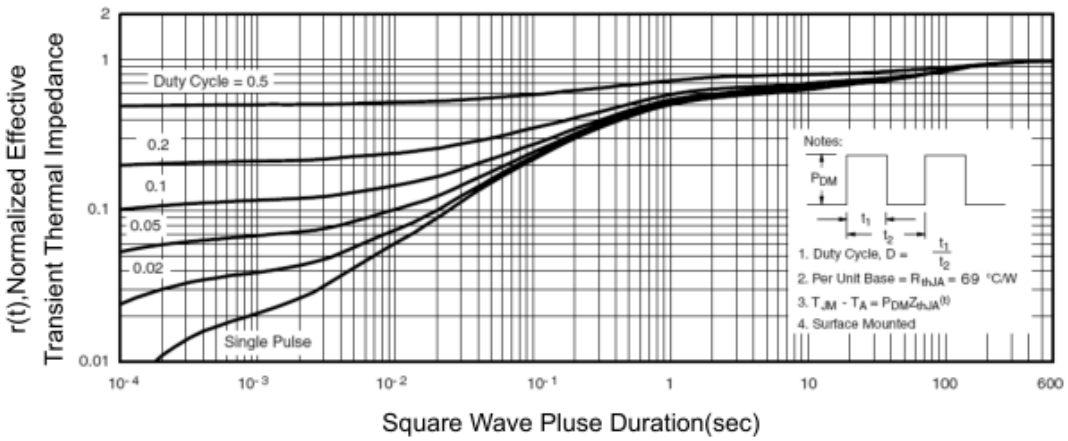
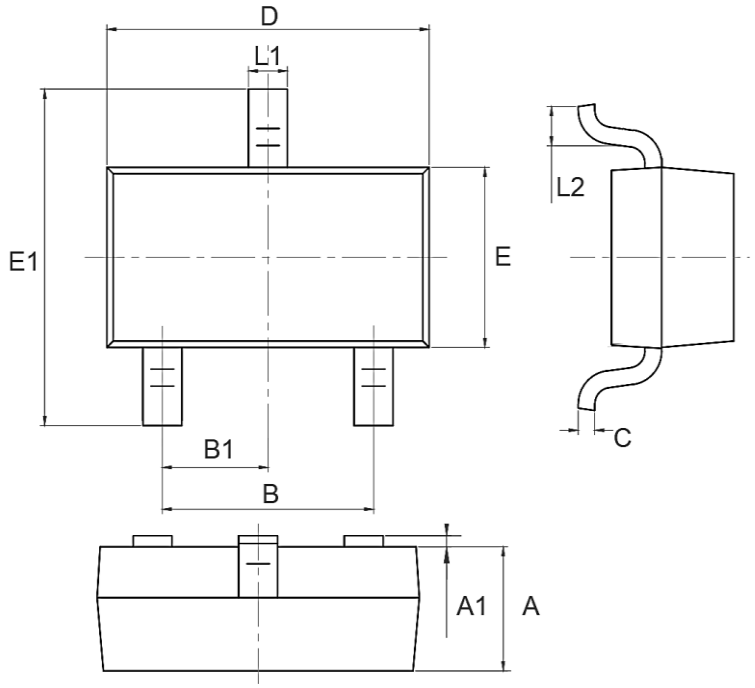


Figure 12 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-SOT23L-Single



Symbol	Dim in mm		
	min	Typ	max
A	0.9	1	1.1
A1	0	0.05	0.1
B	1.8	1.9	2
B1	0.95TYP		
C	0.08	0.115	0.15
D	2.8	2.9	3
E	1.2	1.3	1.4
E1	2.25	2.4	2.55
L1	0.3	0.4	0.5
L2	0.2	0.35	0.5

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-18V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2020/9/8	Initial release
REV1.1	2024/1/16	BVdss≥18V