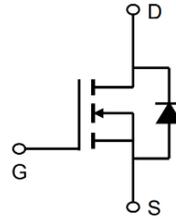


650V N-Channel Enhancement Mode MOSFET

Description

The AP1N65MSI-H is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

$V_{DS} = 650V$ $I_D = 1.0A$

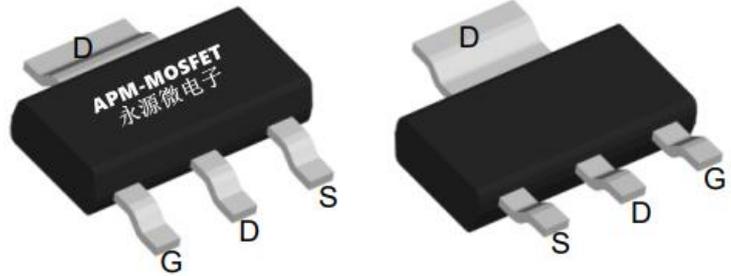
$R_{DS(ON)} < 12\Omega$ @ $V_{GS}=10V$ (Type: 9.5 Ω)

Application

LED

Top View

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP1N60MSI-H	SOT223-3L	AP1N60MSI XXX YYYY	3000

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	650	V
I_D	Continuous Drain Current	1.0	A
I_{DM}	Pulsed Drain Current (note1)	0.6	A
V_{GS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (note2)	14	mJ
P_D	Power Dissipation ($T_c = 25^\circ C$)	20	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	$-55 \sim +150$	$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	5	$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	125	$^\circ C/W$

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Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	650	720	--	V
VGS(th)	Gate-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	3.2	5.0	5.8	V
RDS(on)	Drain-Source On-Resistance	V _{GS} = 10V, I _D = 0.5A	--	9.5	12	Ω
IDSS	Zero Gate Voltage Drain Current	V _{DS} =650V, V _{GS} = 0V, T _J = 25°C	--	--	1	μA
		V _{DS} =520V, V _{GS} = 0V, T _J = 125°C	--	--	100	
IGSS	Gate-Source Leakage	V _{GS} = ±30V	--	--	±100	nA
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} =25V, f=1.0MHz	--	139	--	pF
C _{oss}	Output Capacitance		--	17	--	
C _{rss}	Reverse Transfer Capacitance		--	2.0	--	
Q _g	Total Gate Charge	V _{DD} =350V, I _D =1.0A, V _{GS} =10V	--	5.3	--	nC
Q _{gs}	Gate-Source Charge		--	0.7	--	
Q _{gd}	Gate-Drain Charge		--	2.6	--	
td(on)	Turn-on Delay Time	V _{DD} =350V, I _D =1.0A, R _G =25Ω	--	6	--	ns
t _r	Turn-on Rise Time		--	4.5	--	
td(off)	Turn-off Delay Time		--	27	--	
t _f	Turn-off Fall Time		--	16	--	
I _s	Continuous Body Diode Current	T _C =25°C	--	--	1.0	A
ISM	Pulsed Diode Forward Current		--	--	3.6	
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _s =1.0A, di _f /dt = 100A/μs	--	65	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.53	--	μC
V _{SD}	Body Diode Voltage	T _J = 25°C, I _{SD} = 0.8A, V _{GS} = 0V	--	--	1.5	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

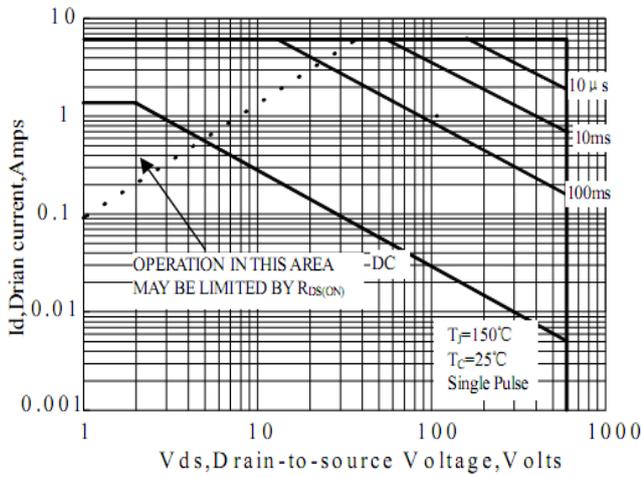


Figure1. Maximum Forward Bias Safe Operating Area

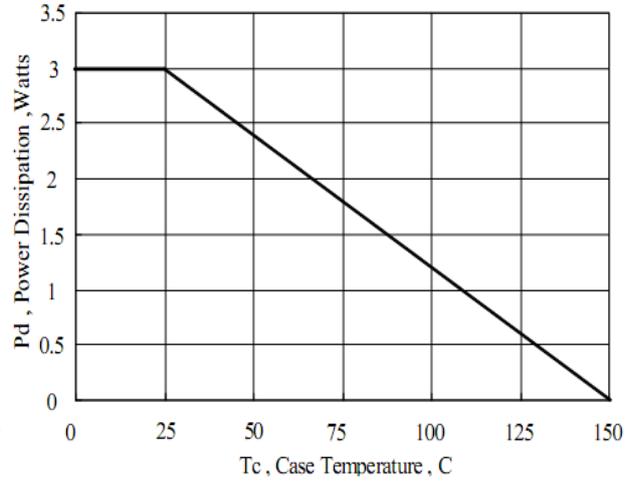


Figure2. Maximum Power Dissipation vs Case Temperature

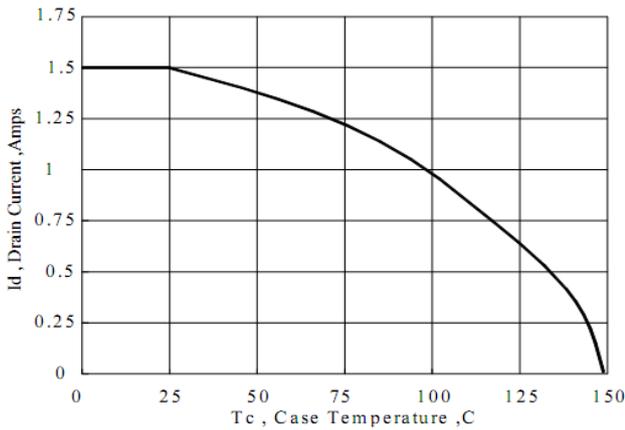


Figure 3 Maximum Continuous Drain Current vs Case Temperature

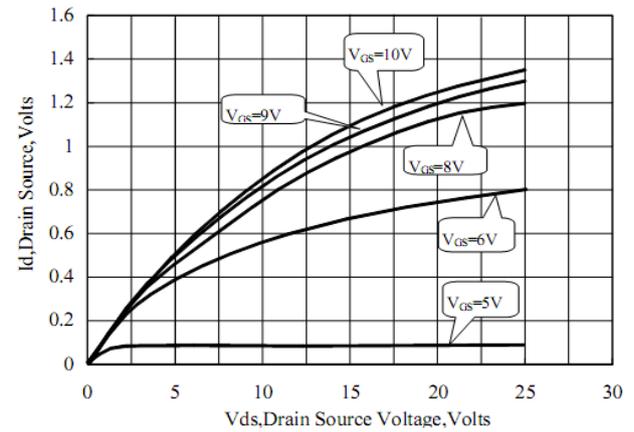


Figure 4 Typical Output Characteristics

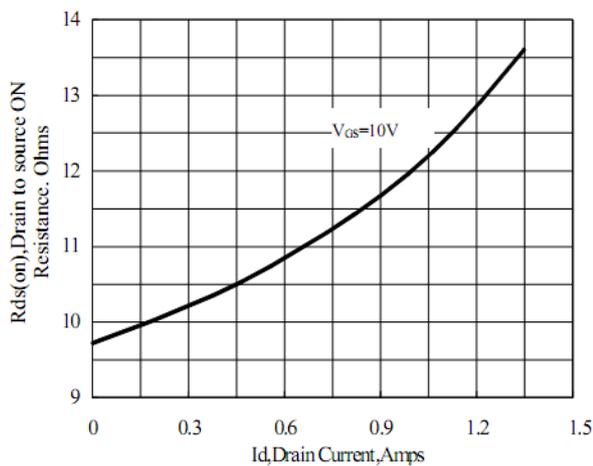


Figure 5 Typical Drain to Source ON Resistance vs Drain Current

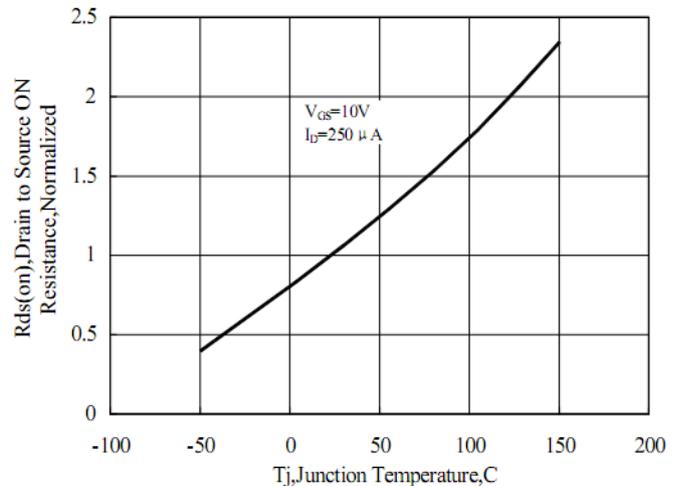


Figure 6 Typical Drain to Source on Resistance vs Junction Temperature



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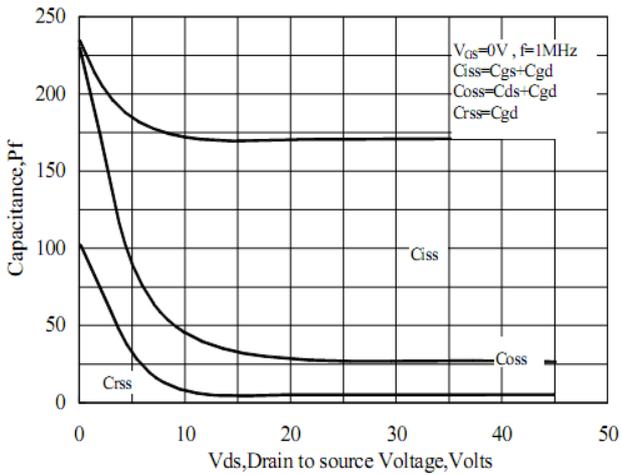


Figure 7 Typical Capacitance vs Drain to Source Voltage

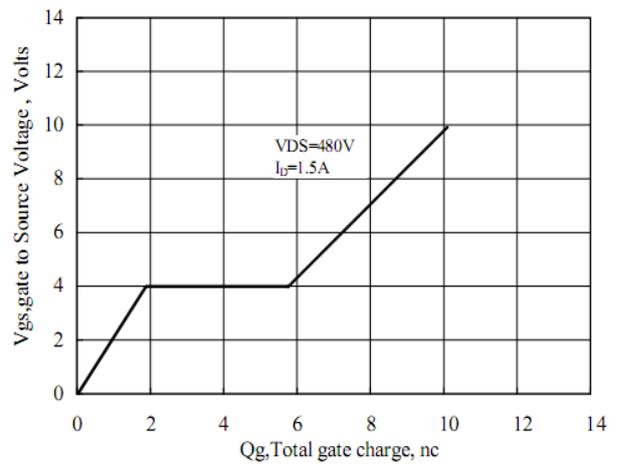


Figure 8 Typical Gate Charge vs Gate to Source Voltage

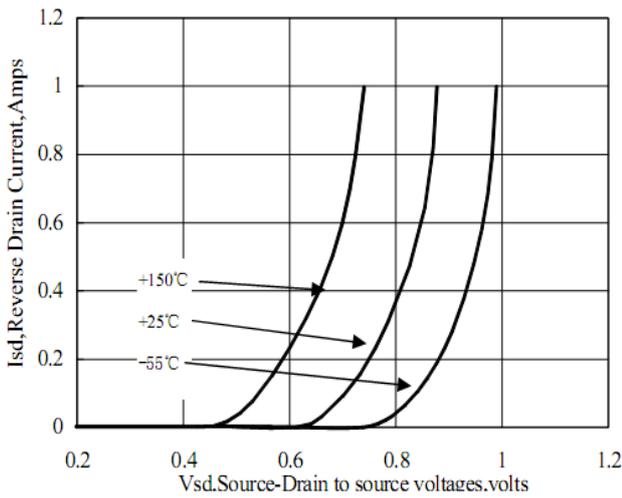


Figure 9 Typical Body Diode Transfer Characteristics

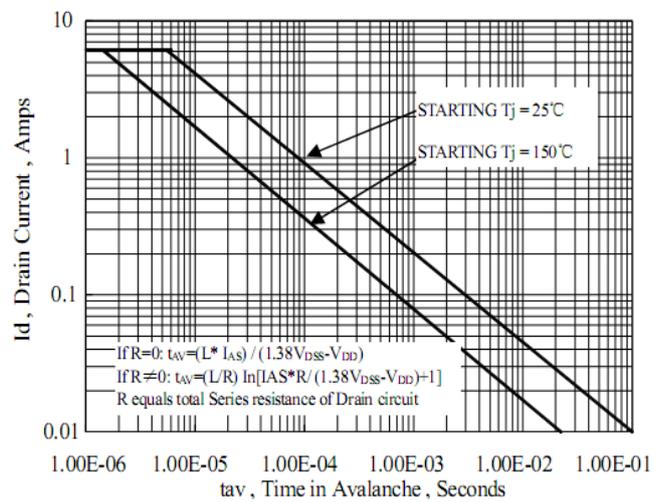


Figure 10 Unclamped Inductive Switching Capability

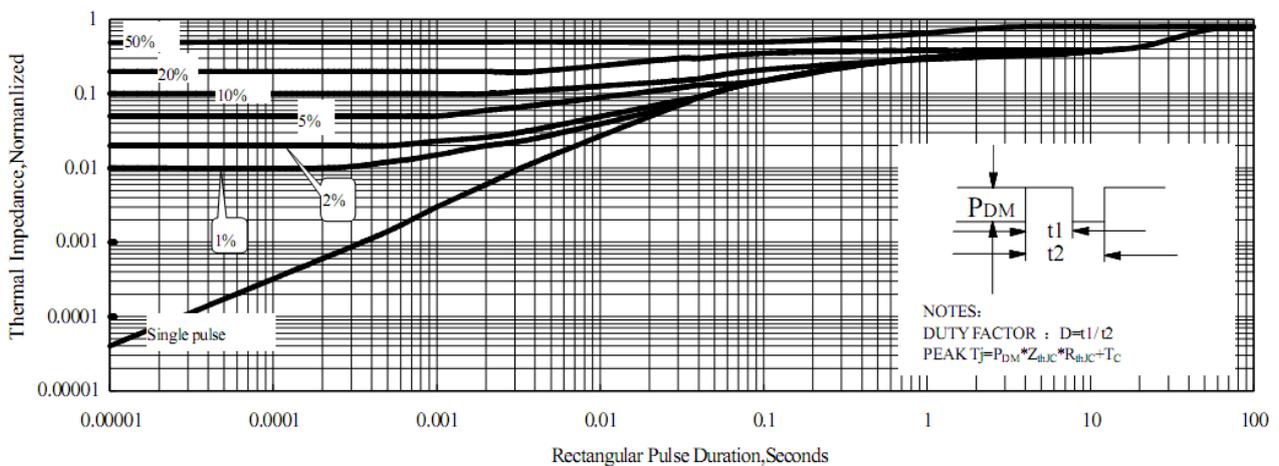
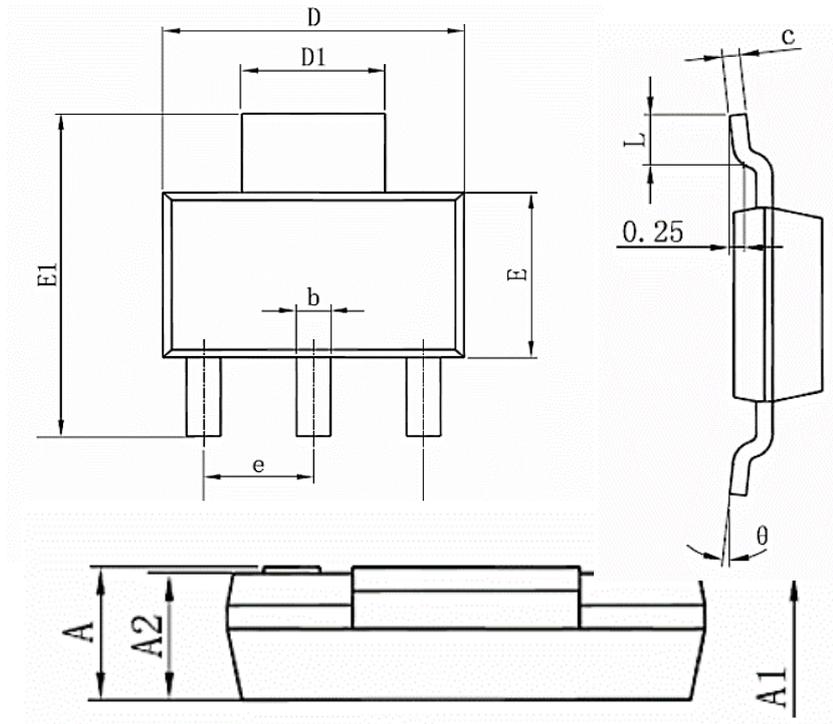


Figure 11 Maximum Effective Thermal Impedance , Junction to Case

Package Mechanical Data:SOT223-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.52	1.8	0.06	0.049
A1	0.000	0.100	0.000	0.004
A2	1.5	1.7	0.059	0.045
b	0.66	0.82	0.026	0.032
c	0.25	0.35	0.010	0.014
D	6.2	6.4	0.244	0.252
D1	2.9	3.1	0.114	0.122
E	3.3	3.7	0.130	0.146
E1	6.83	7.07	0.269	0.278
e	2.300(BSC)		0.037(BSC)	
e1	4.500	4.700	0.177	0.185
L	0.900	1.15	0.035	0.045
theta	0°	10°	0°	10°

650V N-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2023/8/29	Initial release

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