

30V N+P-Channel Enhancement Mode MOSFET

Description

The AP15G03DF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a

Battery protection or in other Switching application.

General Features

$V_{DS} = 30V$ $I_D = 19.3A$

$R_{DS(ON)} < 13m\Omega$ @ $V_{GS}=10V$ (Type: 10m Ω)

$V_{DS} = -30V$ $I_D = -16.5A$

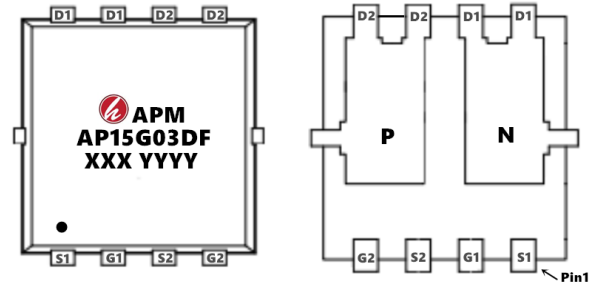
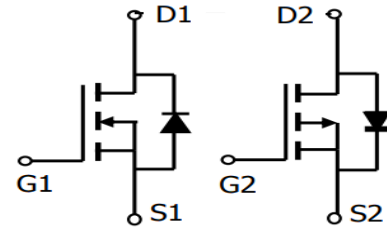
$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=-10V$ (Type: 21m Ω)

Application

Wireless charging

Boost driver

Brushless motor



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15G03DF	PDFN3*3-8L	AP15G03DF XXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	28	-19.7	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	22.5	-17.5	A
I_{DM}	Pulsed Drain Current ²	84	-59.1	A
EAS	Single Pulse Avalanche Energy ³	89	78	mJ
I_{AS}	Avalanche Current	34	33.1	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	46	41.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	5		$^\circ C/W$

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Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	32.5	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.0193	---	V/ $^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=15A$	---	9	13	m Ω
		$V_{GS}=4.5V, I_D=10A$	---	13	16	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-3.97	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	34	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	1.8	---	Ω
Qg	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=15A$	---	9.8	---	nC
Qgs	Gate-Source Charge		---	4.2	---	
Qgd	Gate-Drain Charge		---	3.6	---	
Td(on)	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	4	---	ns
Tr	Rise Time		---	8	---	
Td(off)	Turn-Off Delay Time		---	31	---	
Tf	Fall Time		---	4	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	940	---	pF
Coss	Output Capacitance		---	131	---	
Crss	Reverse Transfer Capacitance		---	109	---	
Is	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	43	A
ISM	Pulsed Source Current ^{2,5}		---	---	112	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V
t _{rr}	Reverse Recovery Time	$I_F=30A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	8.5	---	nS
Q _{rr}	Reverse Recovery Charge		---	2.2	---	nC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=10A$
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Electrical Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	32.5	---	V
ΔBVDSS/ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.022	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-15A	---	21	25	mΩ
		V _{GS} =-4.5V, I _D =-10A	---	33	38	
VGS(th)	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-2 50uA	-1.0	-1.6	-2.5	V
ΔVGS(th)	VGS(th) Temperature Coefficient		---	4.6	---	mV/°C
IDSS	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	-5	
IGSS	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
gfs	Forward Transconductance	V _{DS} =-5V, I _D =-6A	---	17	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-6A	---	12.6	---	nC
Q _{gs}	Gate-Source Charge		---	4.8	---	
Q _{gd}	Gate-Drain Charge		---	4.8	---	
Td(on)	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-6A	---	4.6	---	ns
T _r	Rise Time		---	14.8	---	
Td(off)	Turn-Off Delay Time		---	41	---	
T _f	Fall Time		---	19.6	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	1345	---	pF
C _{oss}	Output Capacitance		---	194	---	
C _{rss}	Reverse Transfer Capacitance		---	158	---	
I _s	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-6.5	A
ISM	Pulsed Source Current ^{2,5}		---	---	-26	A
VSD	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V
t _{rr}	Reverse Recovery Time	IF=-6A, dI/dt=100A/μs, T _J =25°C	---	16.3	---	nS
Q _{rr}	Reverse Recovery Charge		---	5.9	---	nC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3、The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-10A
- 4、The power dissipation is limited by 150°C junction temperature
- 5、The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

N-Typical Characteristics

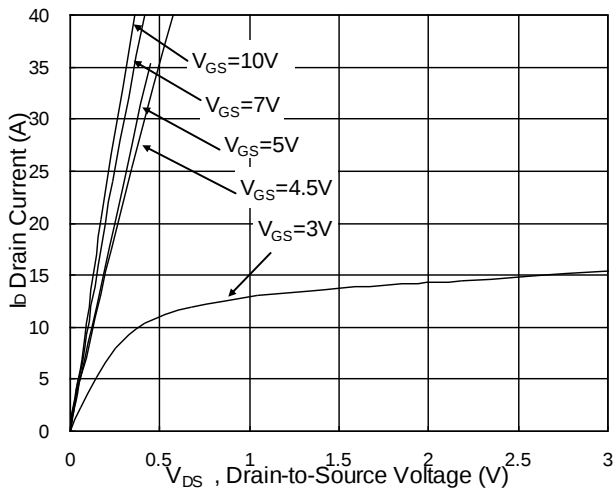


Fig.1 Typical Output Characteristics

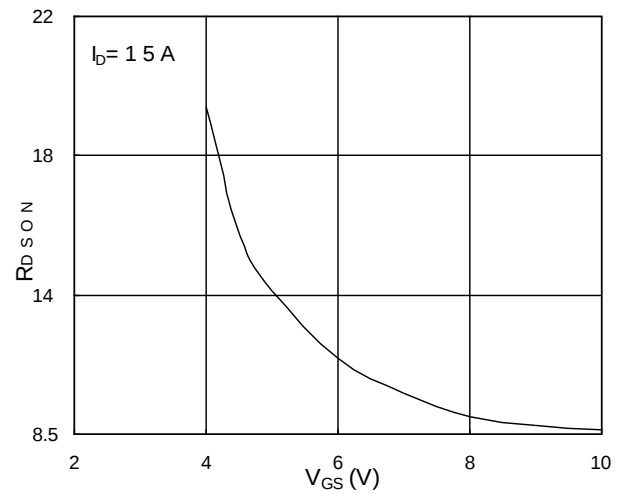


Fig.2 On-Resistance vs. G-S Voltage

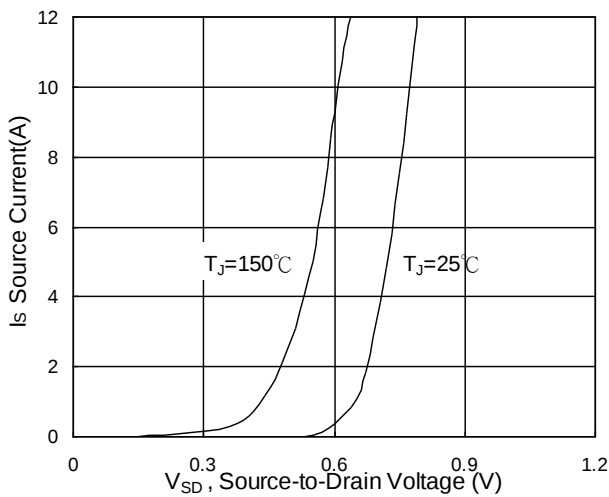


Fig.3 Forward Characteristics of Reverse

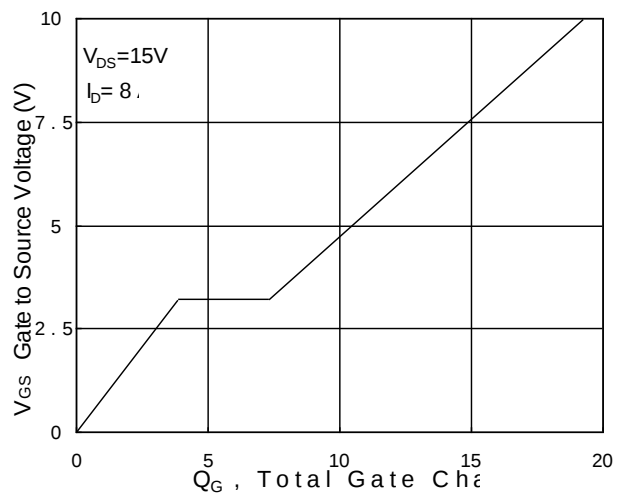


Fig.4 Gate-Charge Characteristics

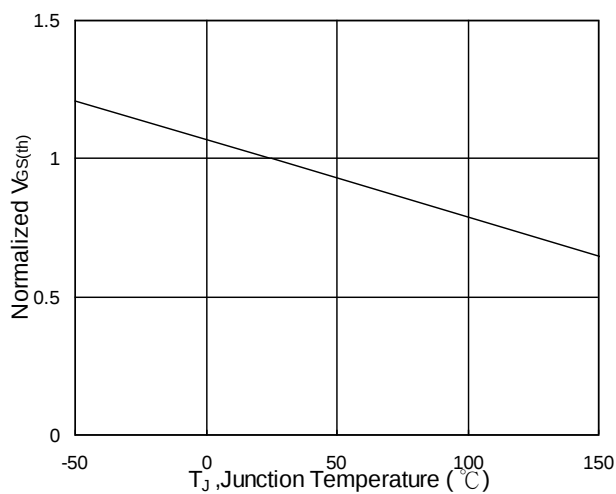


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

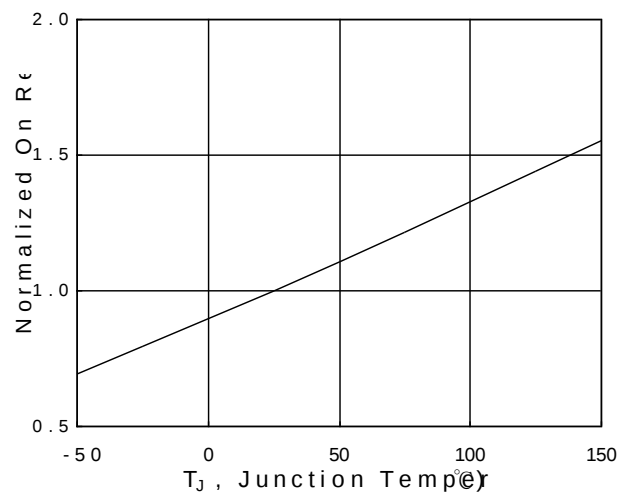


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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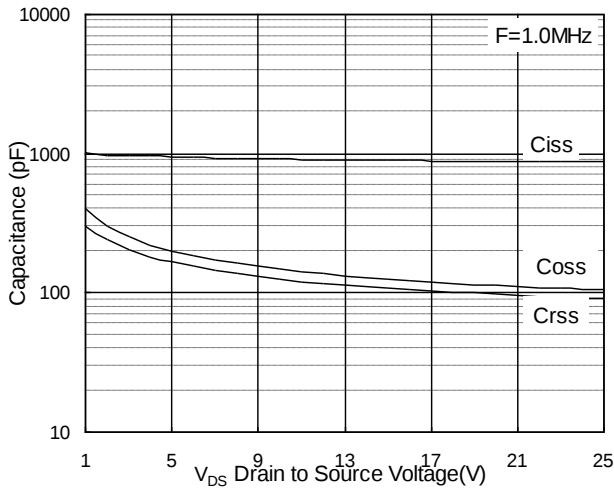


Fig.7 Capacitance

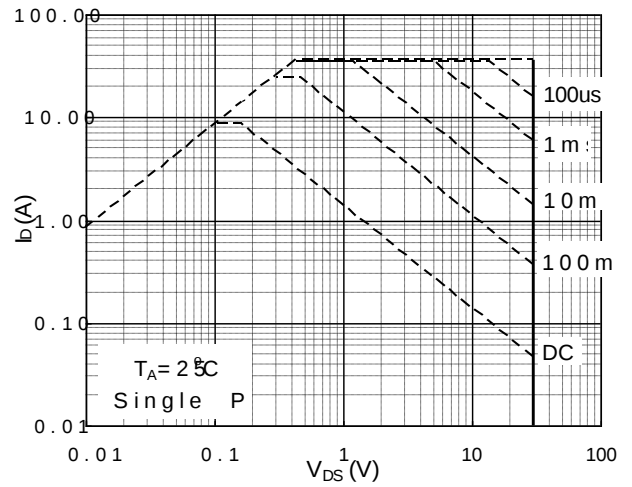


Fig.8 Safe Operating Area

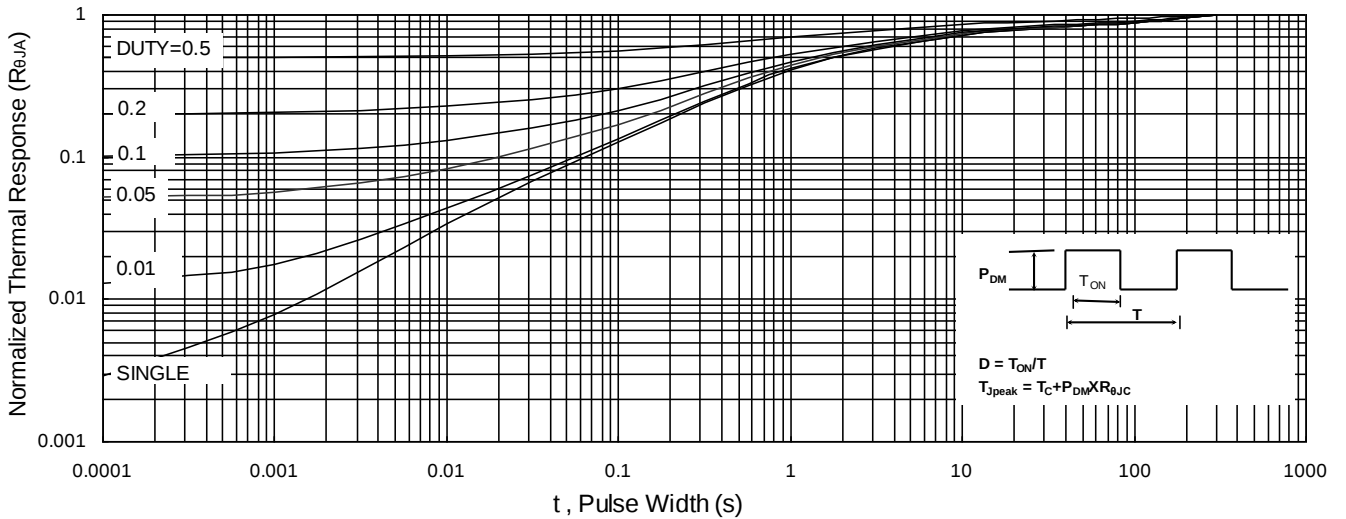


Fig.9 Normalized Maximum Transient Thermal Impedance

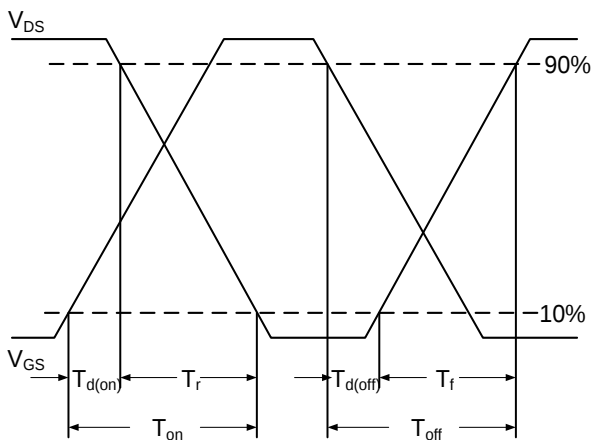


Fig.10 Switching Time Waveform

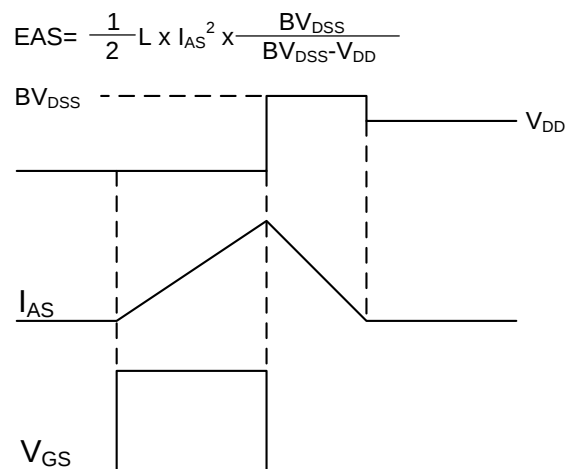


Fig.11 Unclamped Inductive Switching Waveform

P-Typical Characteristics

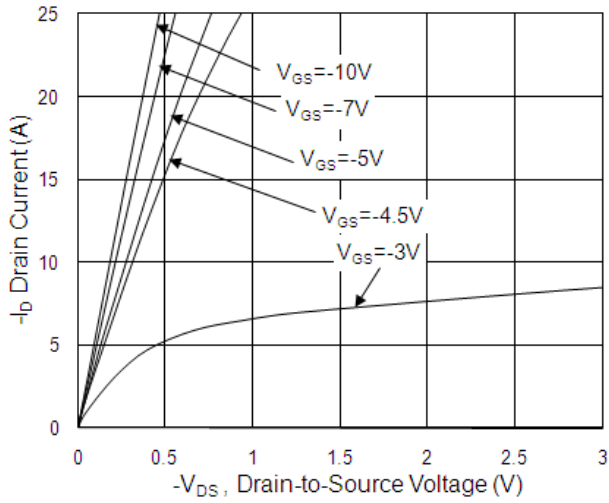


Fig.1 Typical Output Characteristics

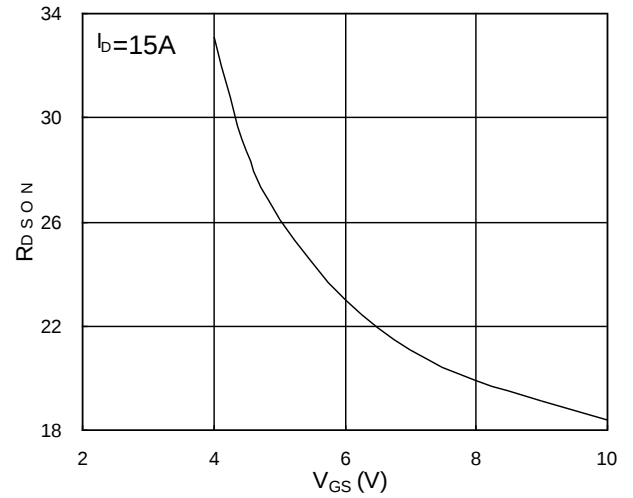


Fig.2 On-Resistance v.s Gate-Source

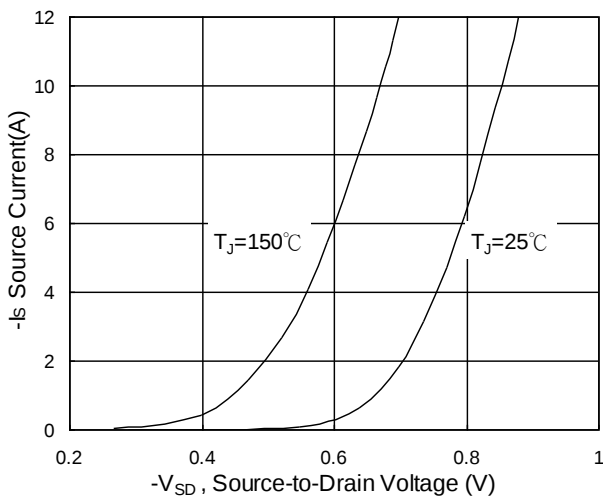


Fig.3 Forward Characteristics of Reverse

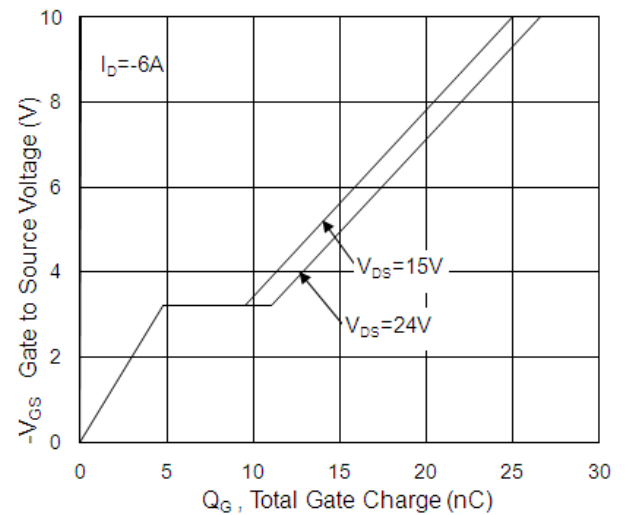


Fig.4 Gate-Charge Characteristics

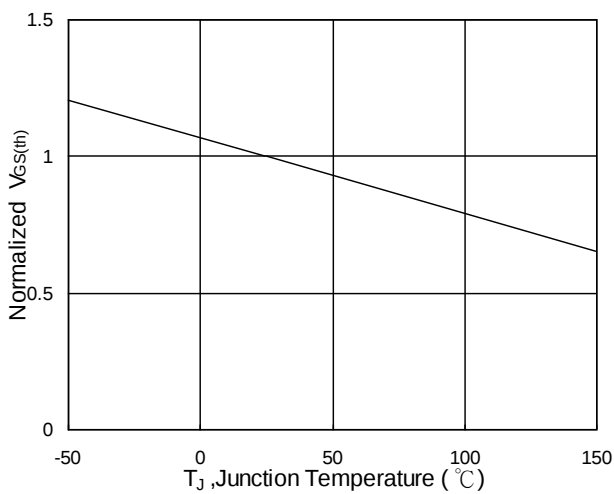


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

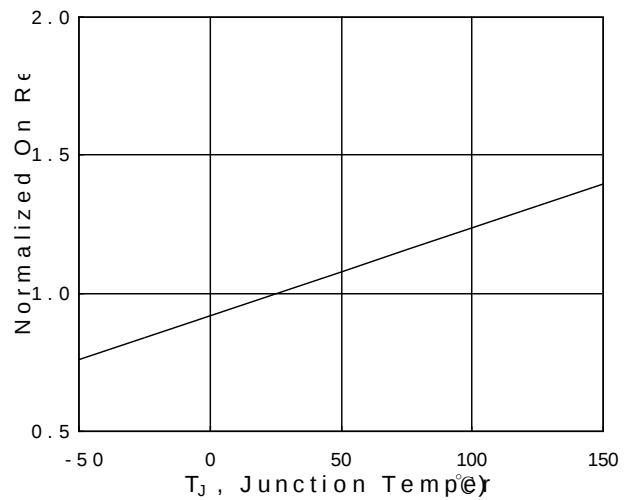


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

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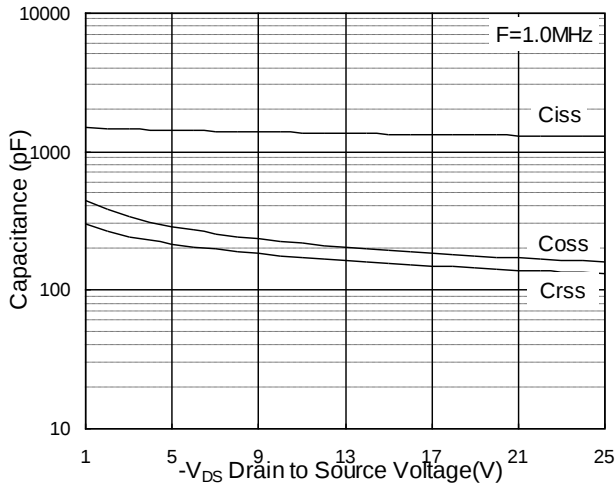


Fig.7 Capacitance

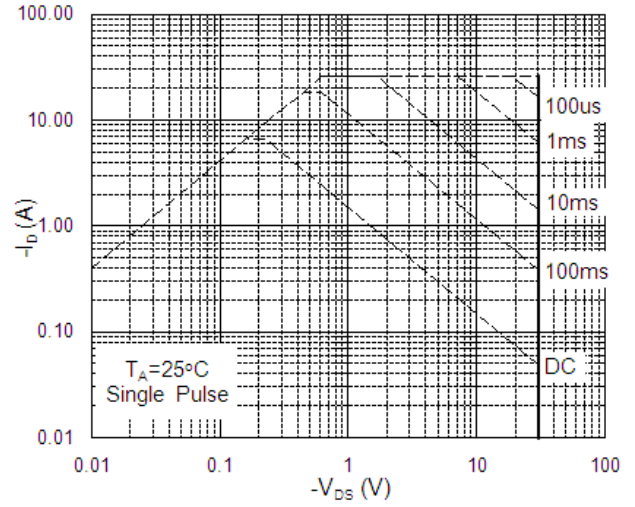


Fig.8 Safe Operating Area

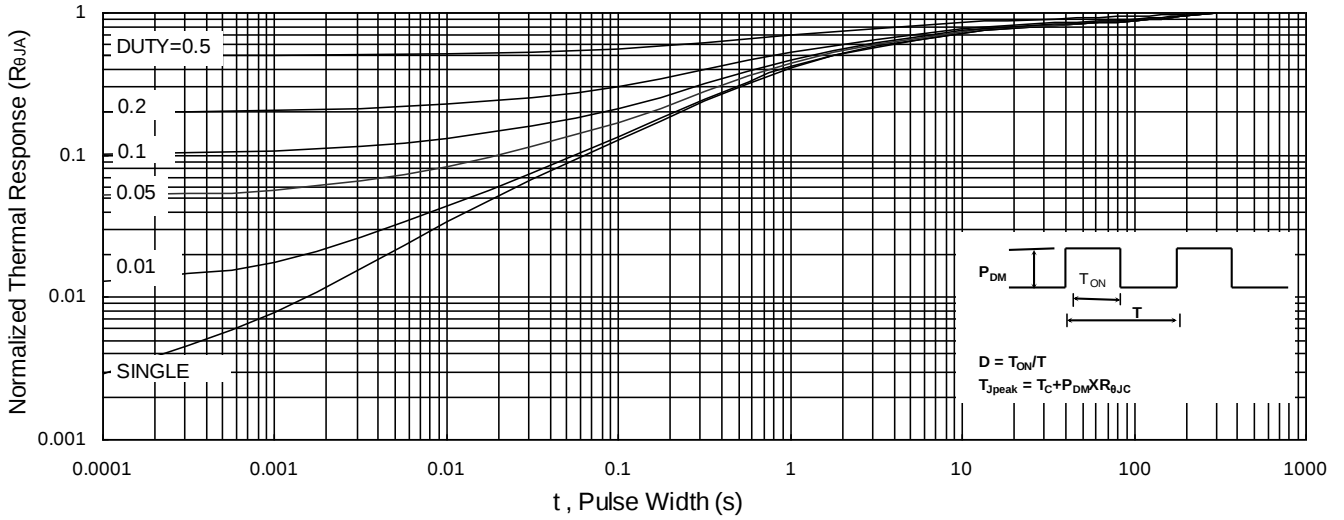


Fig.9 Normalized Maximum Transient Thermal Impedance

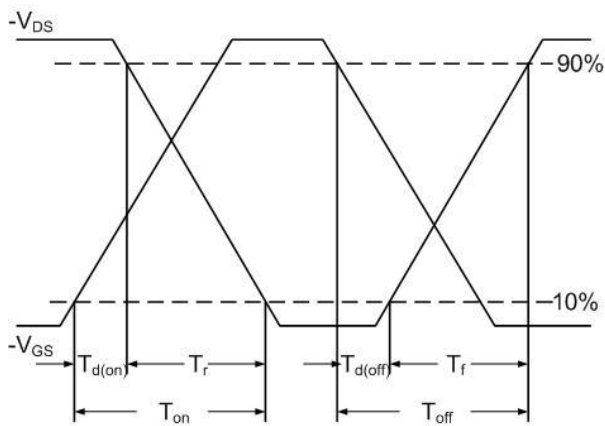


Fig.10 Switching Time Waveform

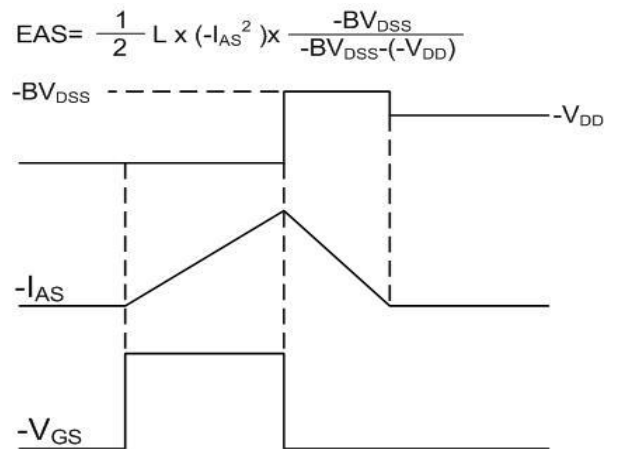
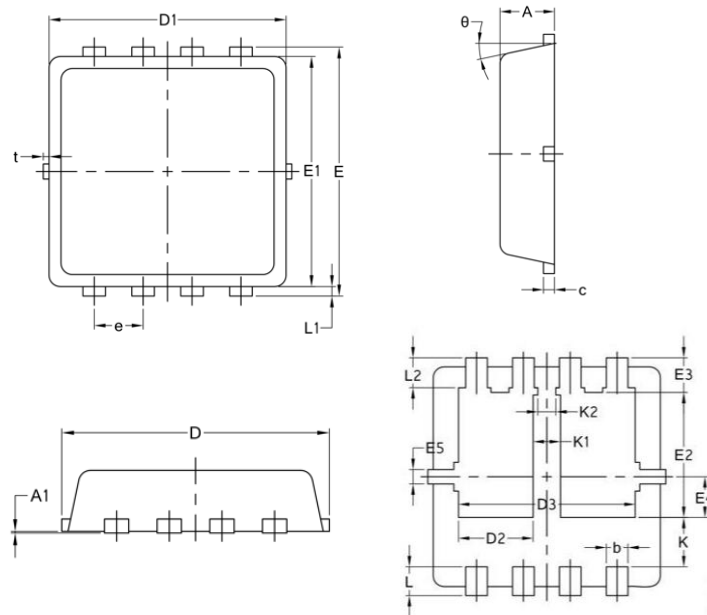


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-DFN3*3-8L-JQ Double



Symbol	Common		
	Mm		
	Min	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.25	0.30	0.39
c	0.14	0.152	0.20
D	3.20	3.30	3.45
D1	3.05	3.15	3.25
D2	0.84	1.04	1.24
D3	2.30	2.45	2.60
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.60	1.74	1.90
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.50	0.69	0.80
K1	0.30	0.38	0.53
K2	0.15	0.25	0.35
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
L2	0.27	0.42	0.57
t	0	0.075	0.13
Φ	10°	12°	14°

30V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2020/10/30	Initial release

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