

40V N+P-Channel Enhancement Mode MOSFET

Description

The AP10G04S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 40V$ $I_D = 9.8A$

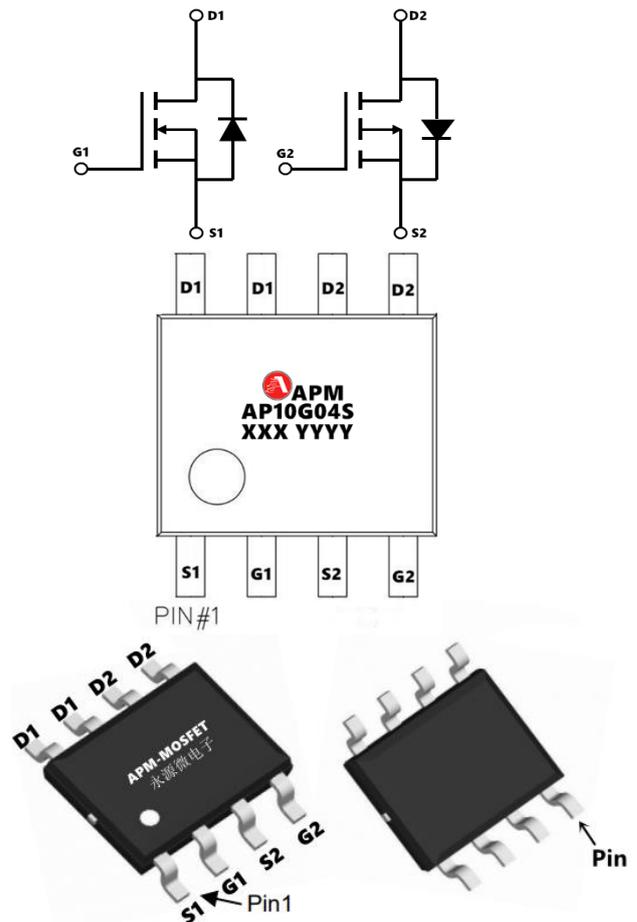
$R_{DS(ON)} < 22m\Omega$ @ $V_{GS}=10V$ (Type: 16m Ω)

$V_{DS} = -40V$ $I_D = -8.5A$

$R_{DS(ON)} < 38m\Omega$ @ $V_{GS}=-10V$ (Type: 31m Ω)

Application

- Wireless charging
- Boost driver
- Brushless motor



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10G04S	SOP-8	AP10G04S XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V _{DS}	Drain-Source Voltage	40	-40	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	9.8	-8.5	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	5.2	-4.8	A
I _{DM}	Pulsed Drain Current ²	23	-22	A
E _{AS}	Single Pulse Avalanche Energy ³	16.2	39	mJ
I _{AS}	Avalanche Current	18	-28	A
P _D @T _A =25°C	Total Power Dissipation ⁴	1.67	1.67	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C
R _{θJA}	Thermal Resistance Junction-Ambient ¹	75		°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	30		°C/W

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N-Channel Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	44	---	V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25\text{ }^\circ\text{C}, I_D=1mA$	---	0.034	---	V/ $^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=5A$	---	16	22	m Ω
		$V_{GS}=4.5V, I_D=4A$	---	18	28	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.56	---	mV/ $^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V, T_J=25\text{ }^\circ\text{C}$	---	---	1	uA
		$V_{DS}=32V, V_{GS}=0V, T_J=55\text{ }^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=5A$	---	14	---	S
Rg	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.6	---	Ω
Qg	Total Gate Charge (4.5V)	$V_{DS}=20V, V_{GS}=4.5V, I_D=5A$	---	5.5	---	nC
Qgs	Gate-Source Charge		---	1.25	---	
Qgd	Gate-Drain Charge		---	2.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=20V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=1A$	---	8.9	---	ns
Tr	Rise Time		---	2.2	---	
Td(off)	Turn-Off Delay Time		---	41	---	
Tf	Fall Time		---	2.7	---	
Ciss	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	593	---	pF
Coss	Output Capacitance		---	76	---	
Crss	Reverse Transfer Capacitance		---	56	---	
Is	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{ Force Current}$	---	---	6.1	A
ISM	Pulsed Source Current ^{2,5}		---	---	23	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25\text{ }^\circ\text{C}$	---	---	1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、 The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=10A$
- 4、 The power dissipation is limited by $150\text{ }^\circ\text{C}$ junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-44	---	V
$\Delta BVDSS/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.02	---	$V/^\circ\text{C}$
RDS(ON)	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-6A$	---	31	38	m Ω
		$V_{GS}=-4.5V, I_D=-3A$	---	43	53	
VGS(th)	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.72	---	$\text{mV}/^\circ\text{C}$
IDSS	Drain-Source Leakage Current	$V_{DS}=-32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
IGSS	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-6A$	---	13	---	S
Qg	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-6A$	---	11.5	---	nC
Qgs	Gate-Source Charge		---	3.5	---	
Qgd	Gate-Drain Charge		---	3.3	---	
Td(on)	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-1A$	---	22	---	ns
Tr	Rise Time		---	15.7	---	
Td(off)	Turn-Off Delay Time		---	59	---	
Tf	Fall Time		---	5.5	---	
Ciss	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	1415	---	pF
Coss	Output Capacitance		---	134	---	
Crss	Reverse Transfer Capacitance		---	102	---	
Is	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-6	A
ISM	Pulsed Source Current ^{2,5}		---	---	-22	A
VSD	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3、 The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-10A$
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

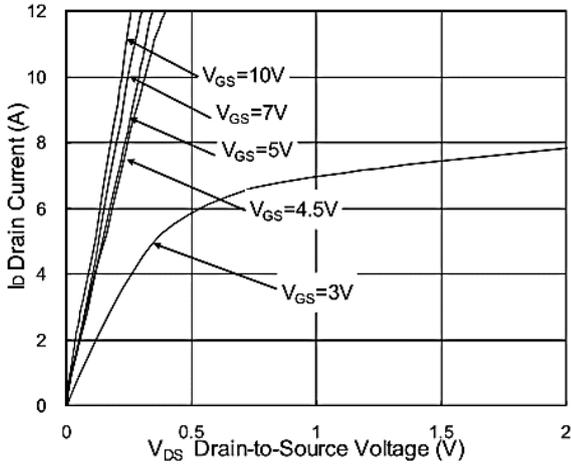


Fig.1 Typical Output Characteristics

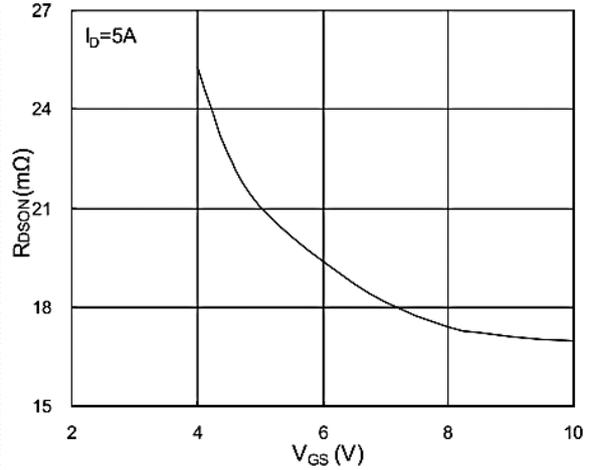


Fig.2 On-Resistance vs. G-S Voltage

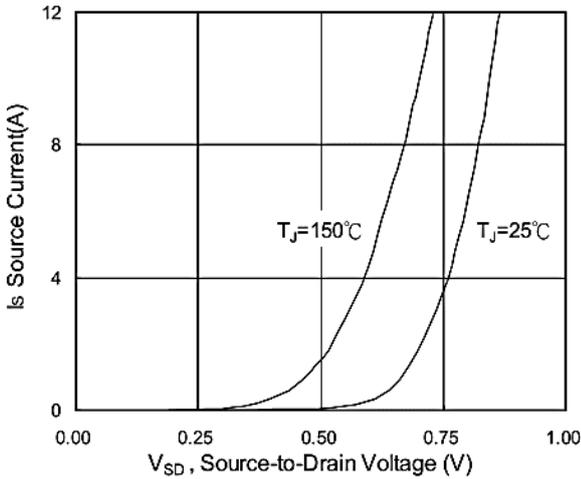


Fig.3 Source Drain Forward Characteristics

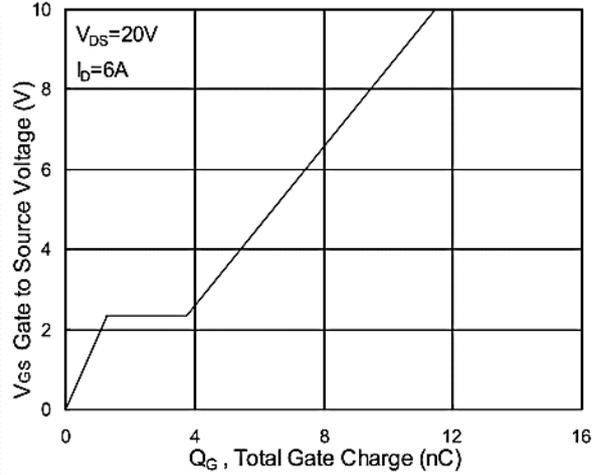


Fig.4 Gate-Charge Characteristics

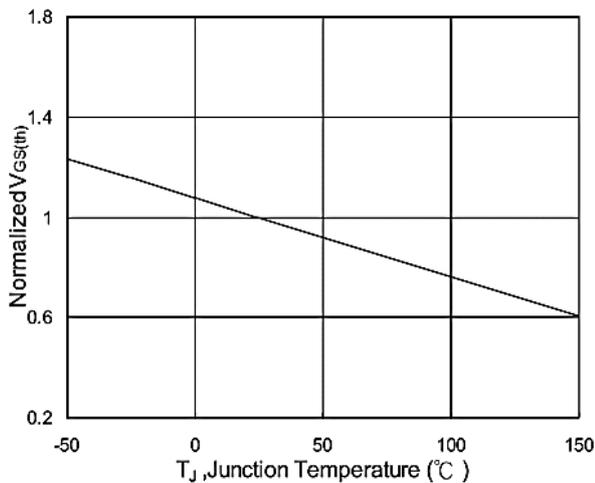


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

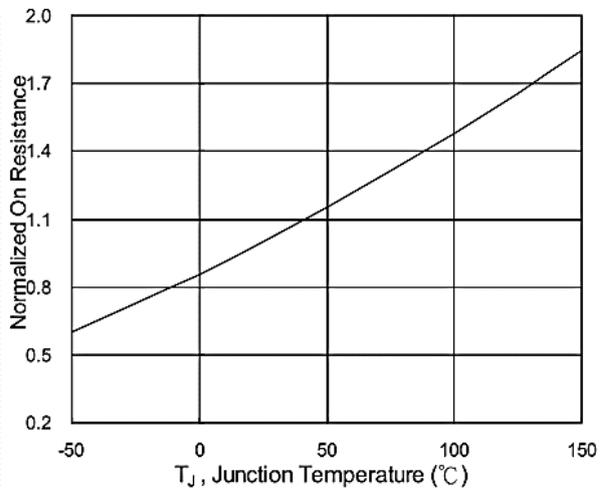


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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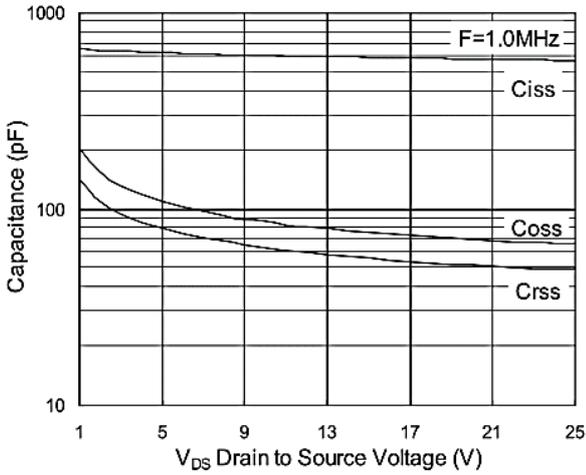


Fig.7 Capacitance

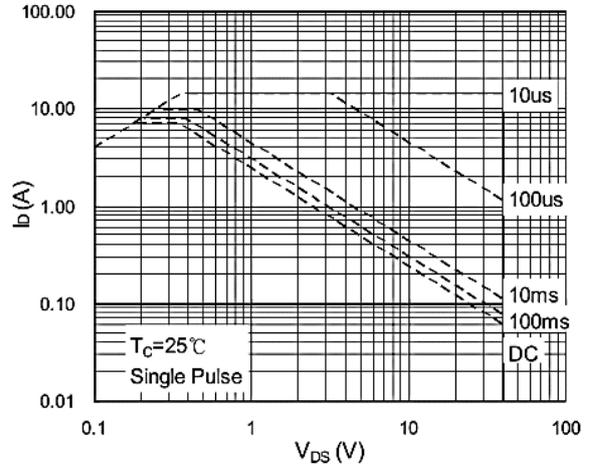


Fig.8 Safe Operating Area

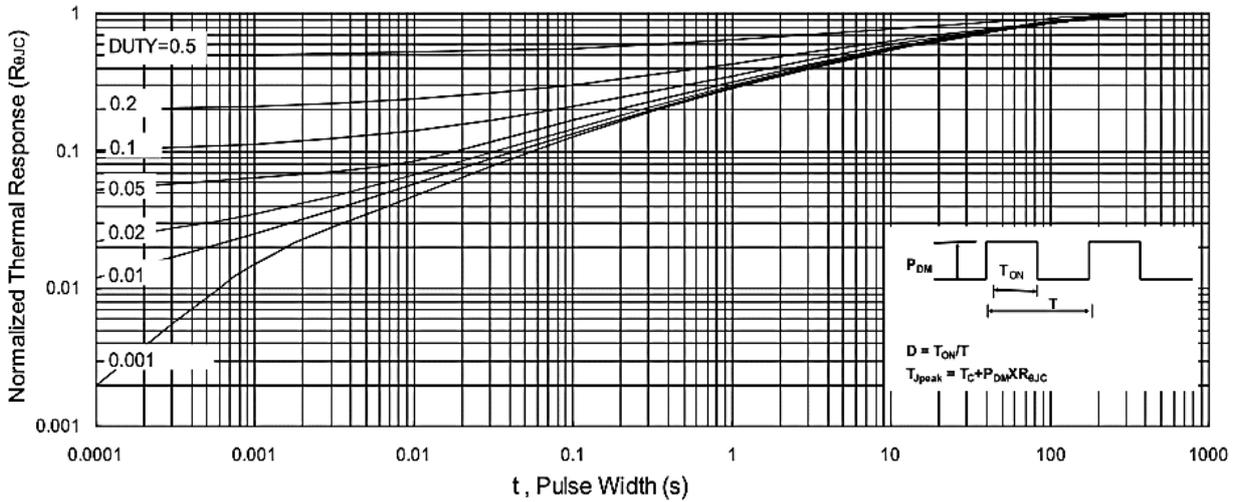


Fig.9 Normalized Maximum Transient Thermal Impedance

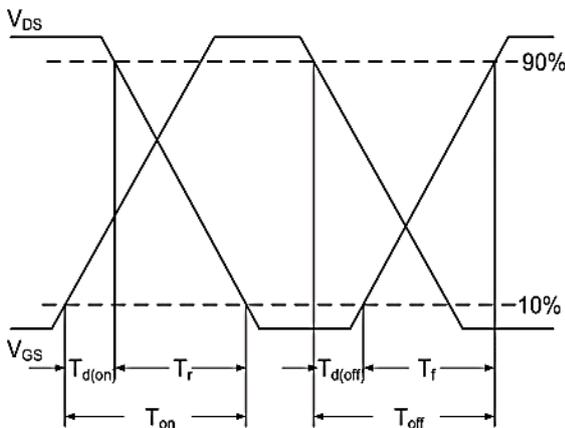


Fig.10 Switching Time Waveform

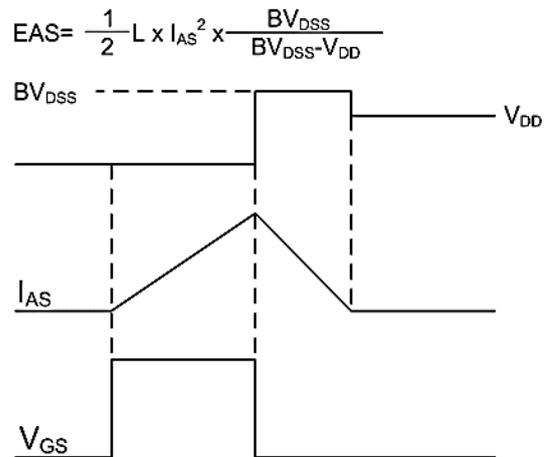


Fig.11 Unclamped Inductive Waveform

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P-Channel Typical Characteristics

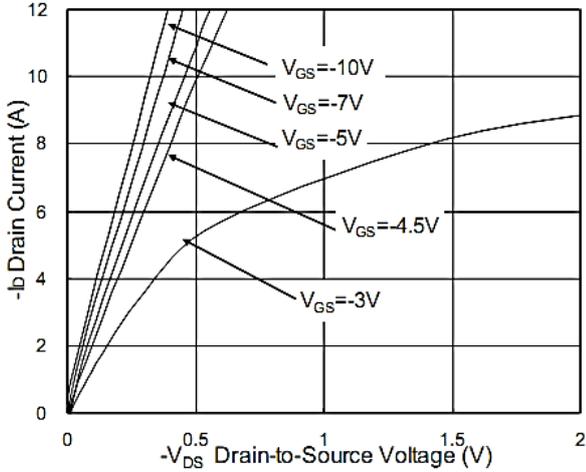


Fig.1 Typical Output Characteristics

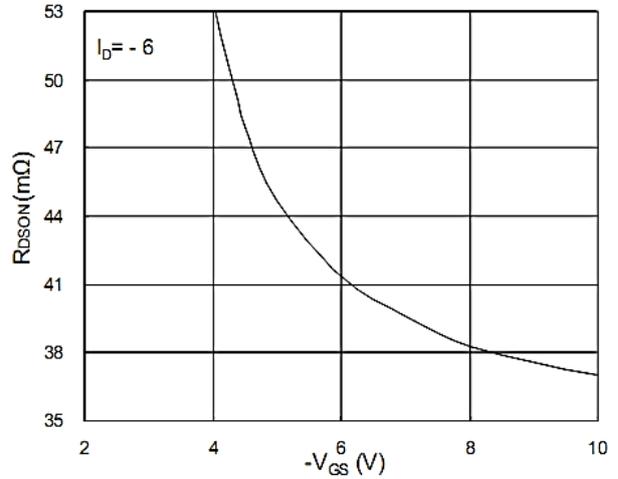


Fig.2 On-Resistance vs. G-S Voltage

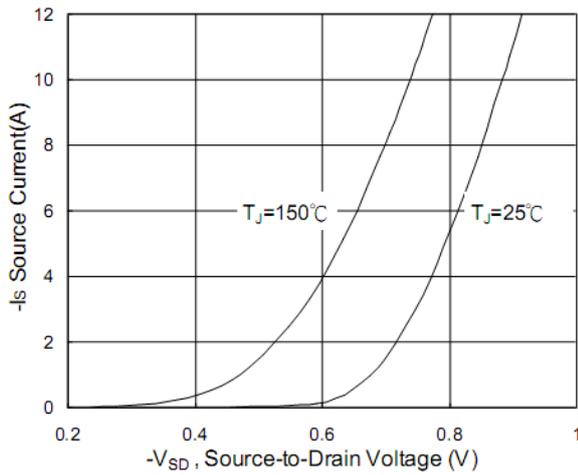


Fig.3 Source Drain Forward Characteristics

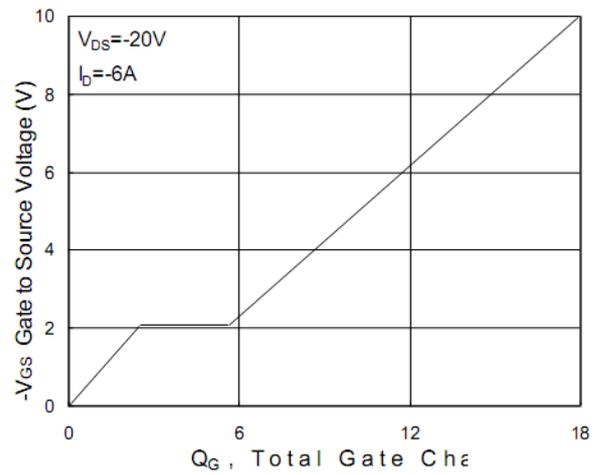


Fig.4 Gate-Charge Characteristics

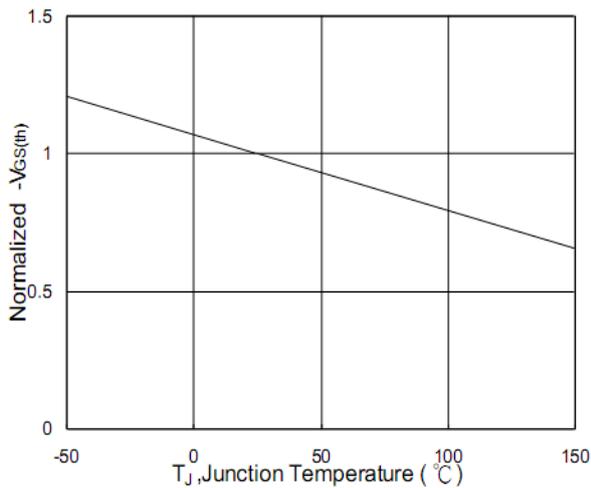


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

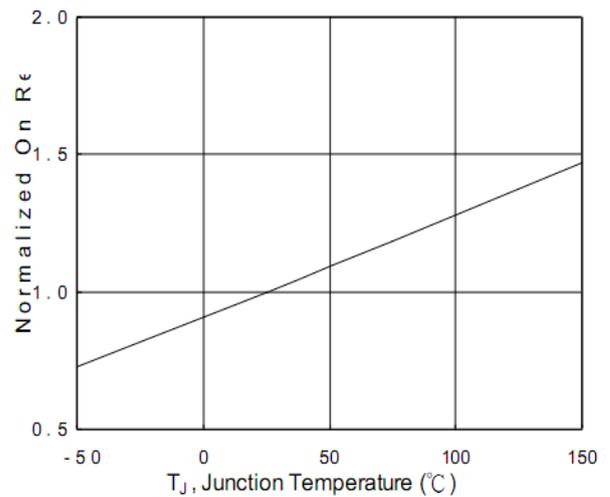


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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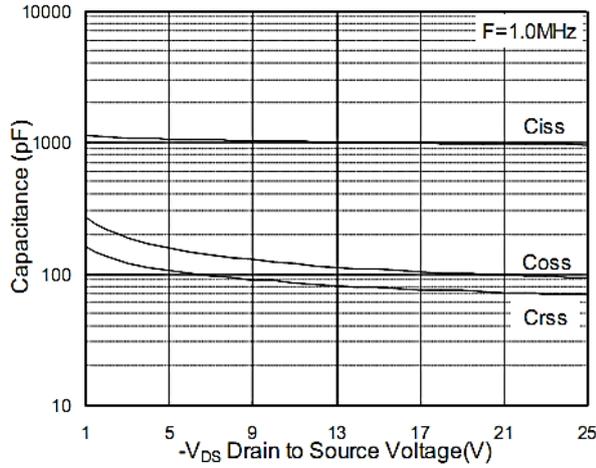


Fig.7 Capacitance

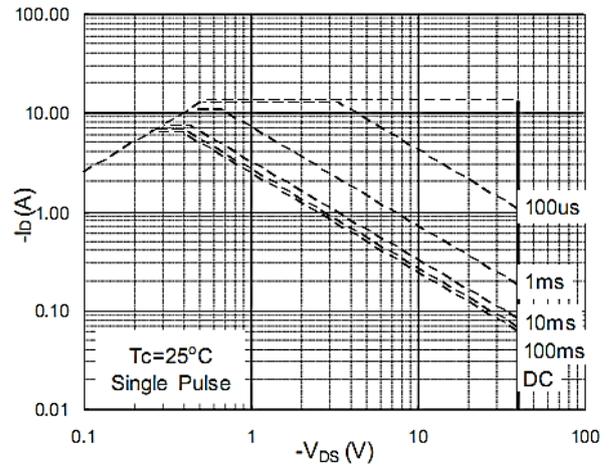


Fig.8 Safe Operating Area

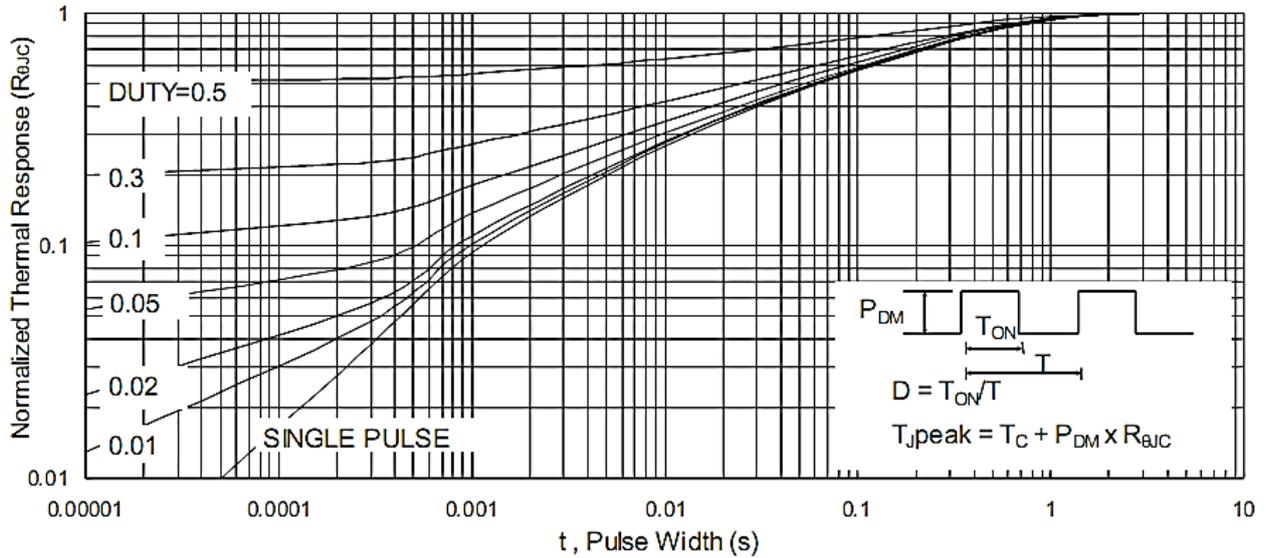


Fig.9 Normalized Maximum Transient Thermal Impedance

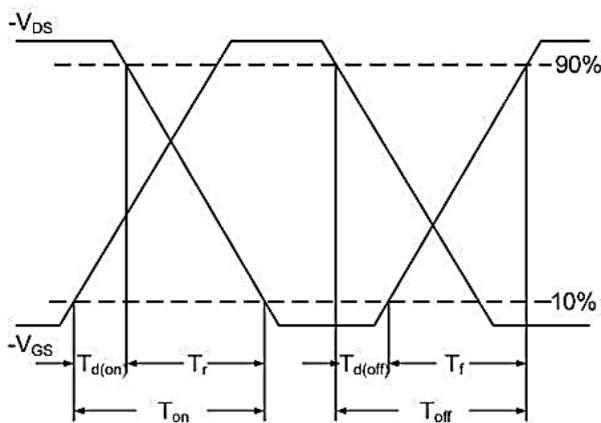


Fig.10 Switching Time Waveform

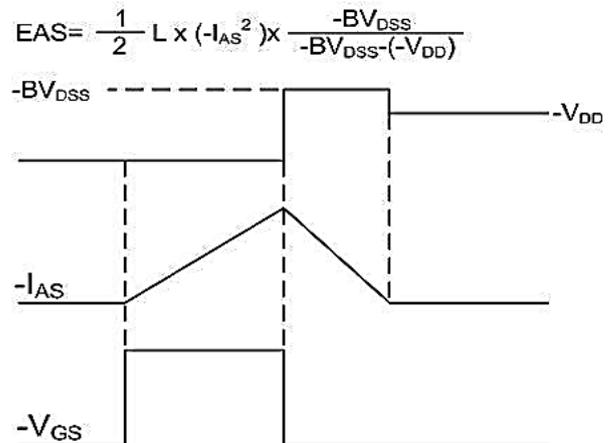
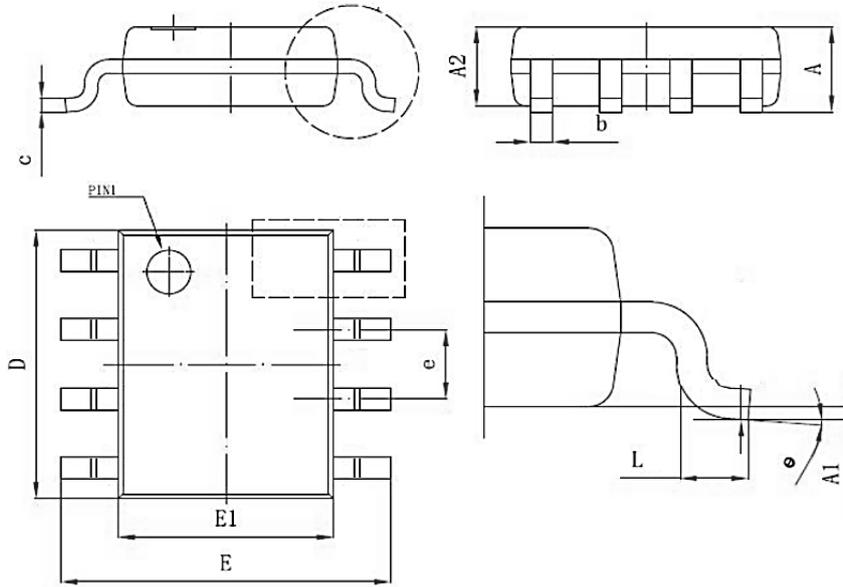


Fig.11 Unclamped Inductive Waveform

Package Mechanical Data-SOP-8L



Symbol	Dim in mm		
	Min	Typ	Max
A	1.35	1.55	1.75
A1	0.02	0.15	0.25
A2	1.425	1.45	1.475
b	0.3	0.4	0.5
c	0.15	0.2	0.25
D	4.8	5	5.2
E	5.8	6	6.2
E1	3.8	4	4.2
e	1.27BSC		
L	0.4		1.27
θ	0°		8°

40V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
REV1.0	2019/5/31	Initial release
REV1.1	2022/1/6	Change format
REV1.2	2024/5/1	Change logo and Reduce Rds

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