

## 30V N+P-Channel Enhancement Mode MOSFET

### Description

The AP10G03S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

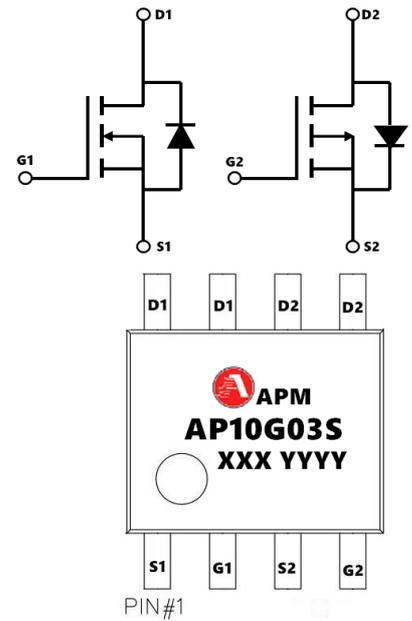
### General Features

$V_{DS} = 30V$   $I_D = 12A$

$R_{DS(ON)} < 12m\Omega$  @  $V_{GS}=10V$

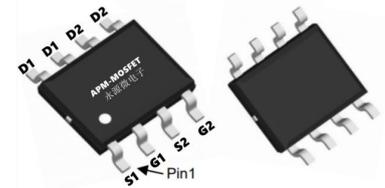
$V_{DS} = -30V$   $I_D = -9.8A$

$R_{DS(ON)} < -25m\Omega$  @  $V_{GS}=10V$



### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10G03S	SOP-8L	AP10G03S XXX YYYY	3000

### Absolute Maximum Ratings ( $T_c=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
$V_{DS}$	Drain-Source Voltage	30	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D @ T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	12	-9.8	A
$I_D @ T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.5	-7.2	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	36	-32	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	24	72	mJ
$I_{AS}$	Avalanche Current	22	-38	A
$P_D @ T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	1.5	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	25	$^\circ C/W$



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### N-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\frac{\partial BV_{DSS}}{\partial T_J}$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	---	0.023	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=8A$	---	---	12	m $\Omega$
		$V_{GS}=4.5V, I_D=6A$	---	---	18	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$\frac{\partial V_{GS(th)}}{\partial T_J}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.08	---	mV/ $^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=8A$	---	24	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.8	---	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=8A$	---	9.63	---	nC
$Q_{gs}$	Gate-Source Charge		---	3.88	---	
$Q_{gd}$	Gate-Drain Charge		---	3.44	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=1.5, I_D=8A$	---	4.2	---	ns
$T_r$	Rise Time		---	8.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	31	---	
$T_f$	Fall Time		---	4	---	
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	940	---	pF
$C_{oss}$	Output Capacitance		---	131	---	
$C_{rss}$	Reverse Transfer Capacitance		---	109	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	9	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	36	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1	V
$t_{rr}$	Reverse Recovery Time	$I_F=8A, \frac{dI}{dt}=100A/\mu s, T_J=25^\circ\text{C}$	---	8	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	2.9	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=21A$
- 4 .The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

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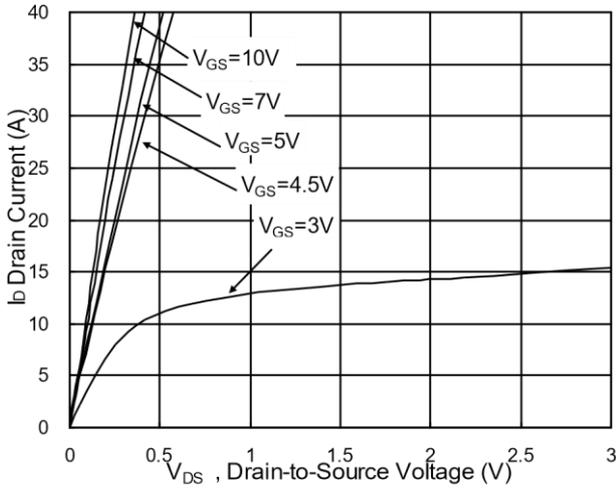
### P-Channel Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$\frac{\partial BV_{DSS}}{\partial T_J}$	BVDSS Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.022	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-6A$	---	---	25	m $\Omega$
		$V_{GS}=-4.5V, I_D=-4A$	---	---	42	
$V_{GS(th)}$	Gate Threshold Voltage		-1.0	---	-2.5	V
$\frac{\partial V_{GS(th)}}{\partial T_J}$	$V_{GS(th)}$ Temperature Coefficient	$V_{GS}=V_{DS}, I_D=-250\mu A$	---	4.6	---	mV/ $^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	$\mu A$
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-6A$	---	17	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	13	---	
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-6A$	---	12.6	---	nC
$Q_{gs}$	Gate-Source Charge		---	4.8	---	
$Q_{gd}$	Gate-Drain Charge		---	4.8	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3, I_D=-6A$	---	4.6	---	ns
$T_r$	Rise Time		---	14.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	41	---	
$T_f$	Fall Time		---	19.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	1345	---	pF
$C_{oss}$	Output Capacitance		---	194	---	
$C_{rss}$	Reverse Transfer Capacitance		---	158	---	
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{Force Current}$	---	---	-6.5	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	-26	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

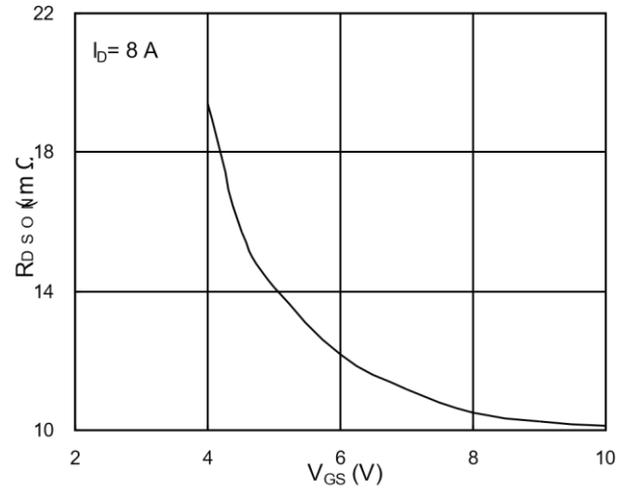
#### Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZcopper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data sh.The power dissipation is limited by ows Max. rating
4. The test condition is  $V_{150^\circ\text{C}}$  junction temperature  $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-30A$
- 5 .The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

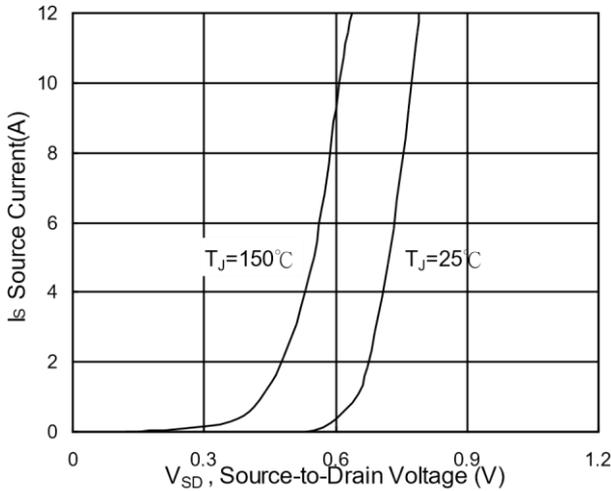
**30V N+P-Channel Enhancement Mode MOSFET**



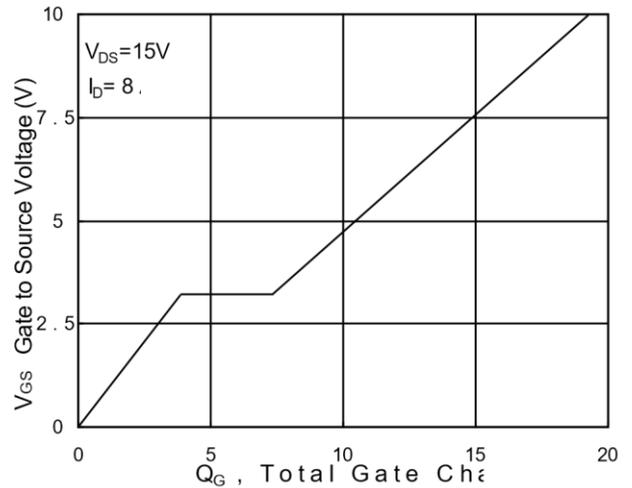
**Fig.1 Typical Output Characteristics**



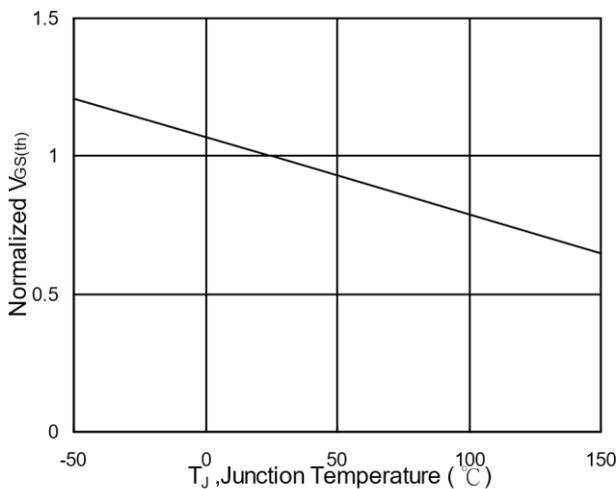
**Fig.2 On-Resistance vs. G-S Voltage**



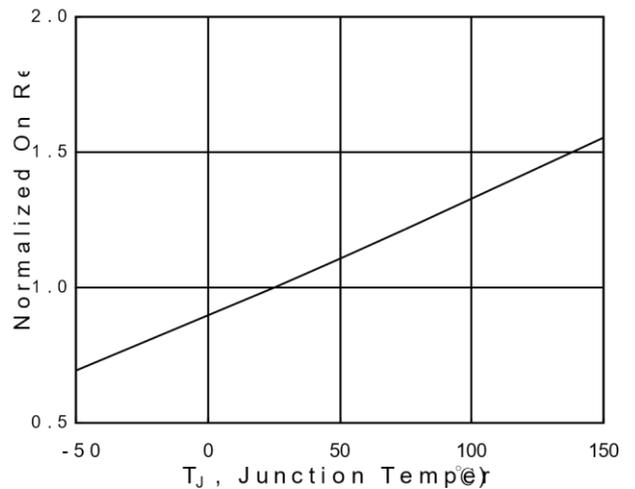
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

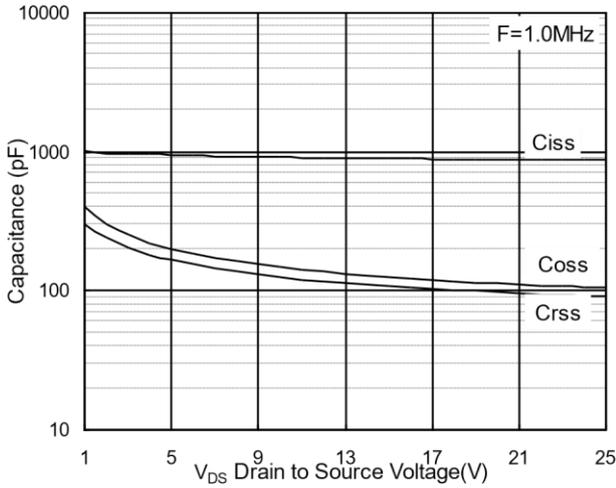


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

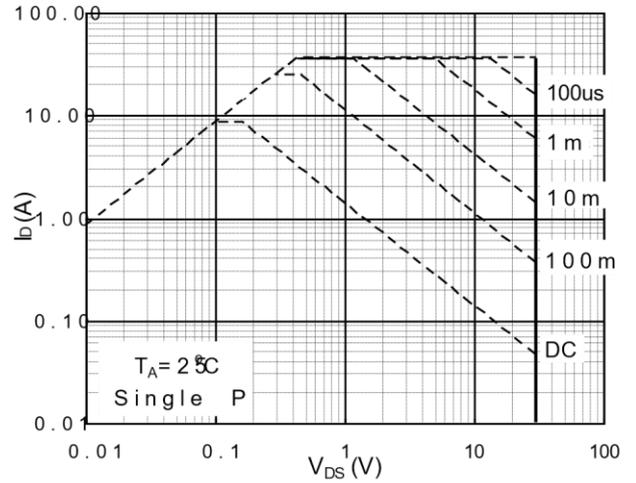


**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

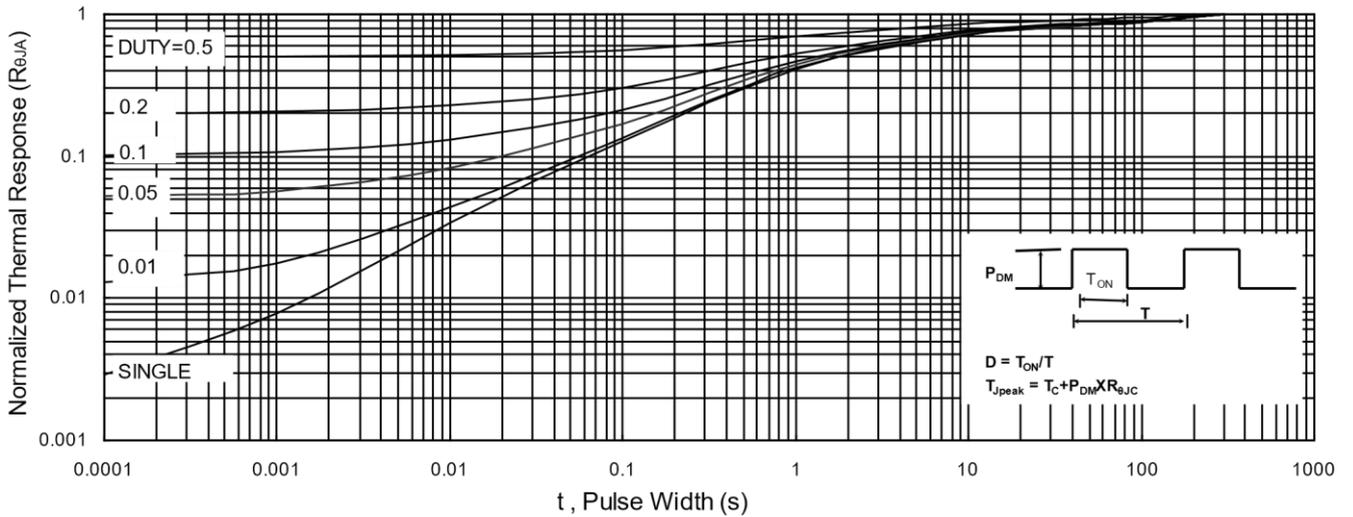
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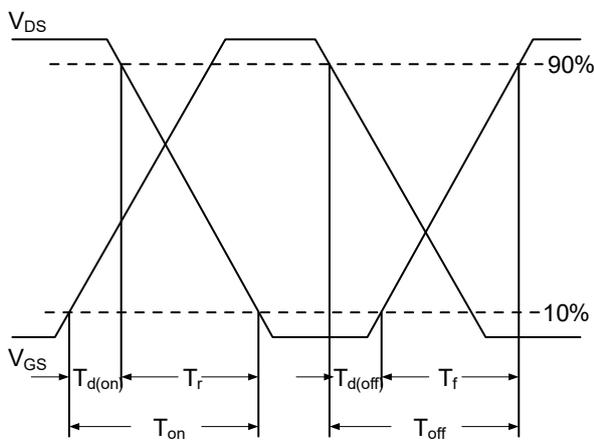
**Fig.7 Capacitance**



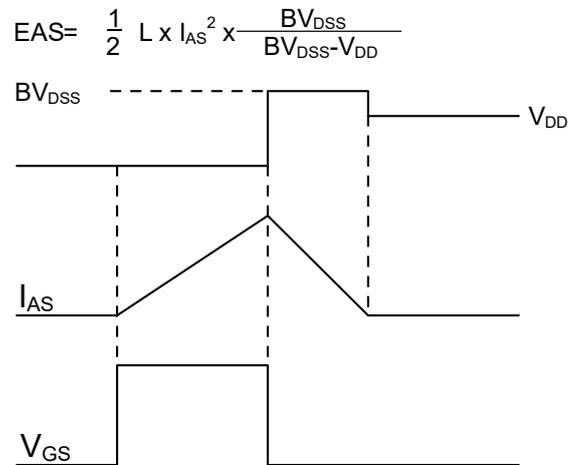
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

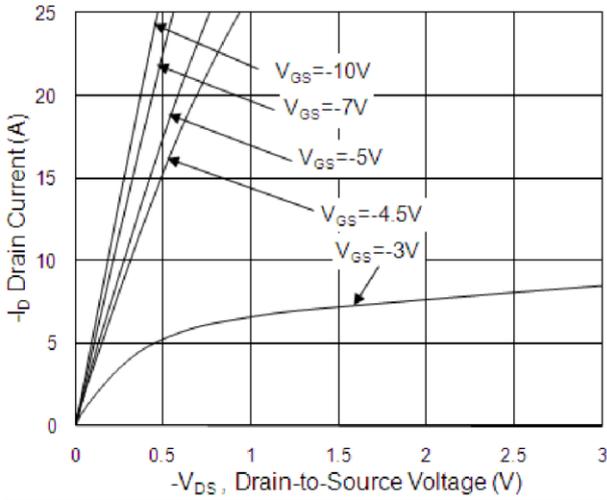


**Fig.10 Switching Time Waveform**

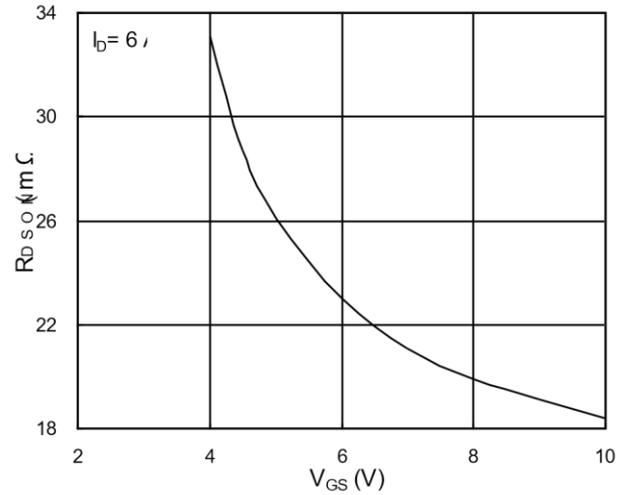


**Fig.11 Unclamped Inductive Switching Waveform**

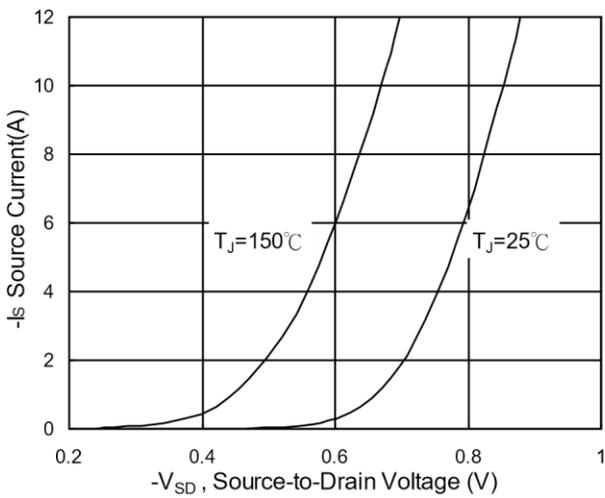
**30V N+P-Channel Enhancement Mode MOSFET**



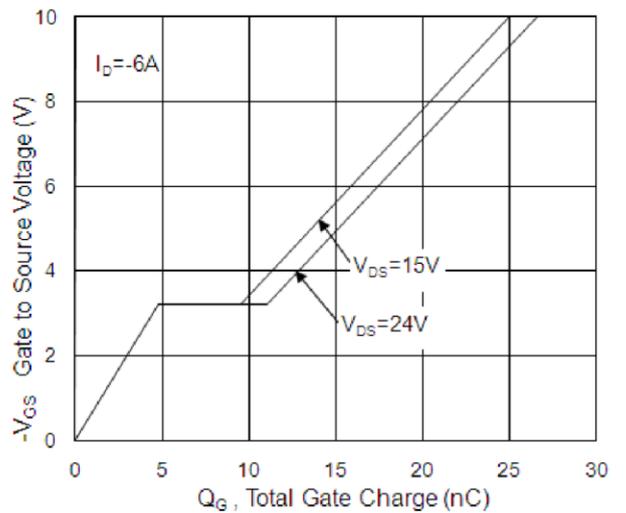
**Fig.1 Typical Output Characteristics**



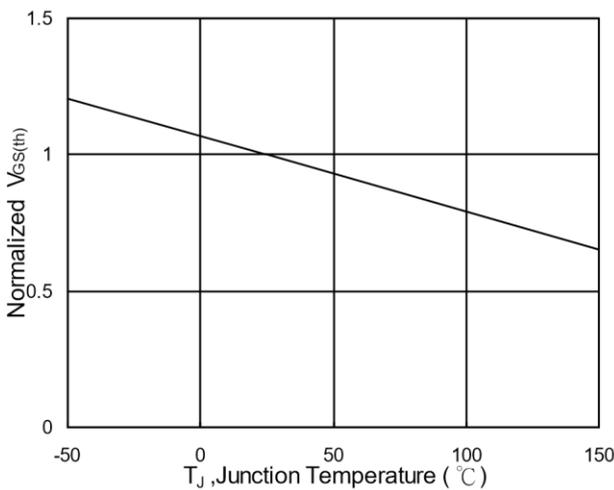
**Fig.2 On-Resistance v.s Gate-Source**



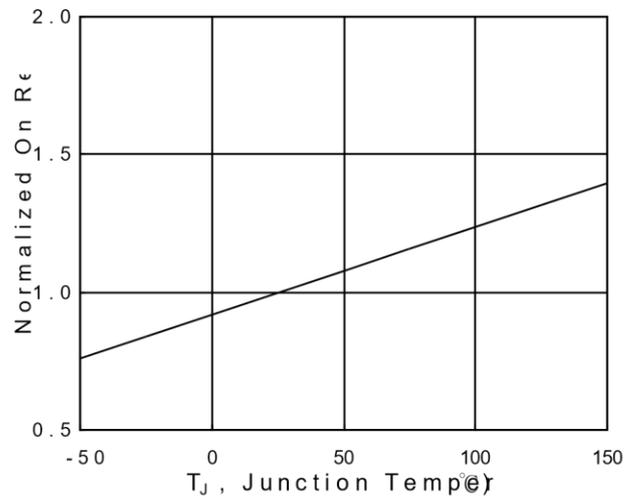
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

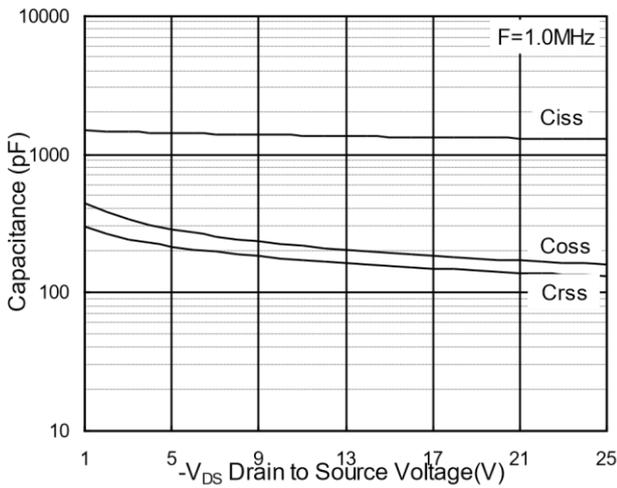


**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**

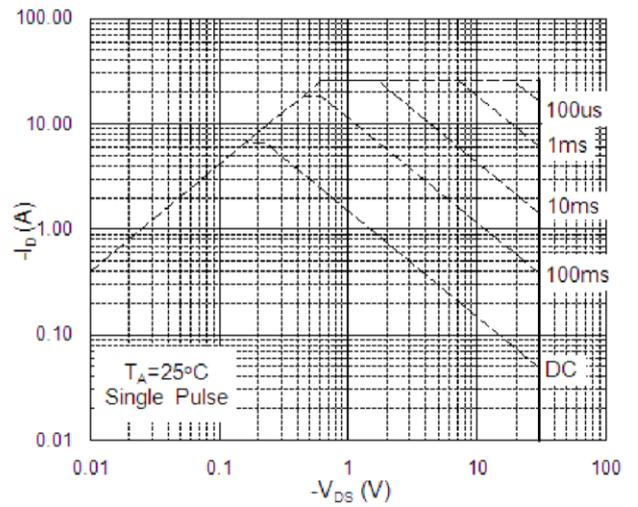


**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**

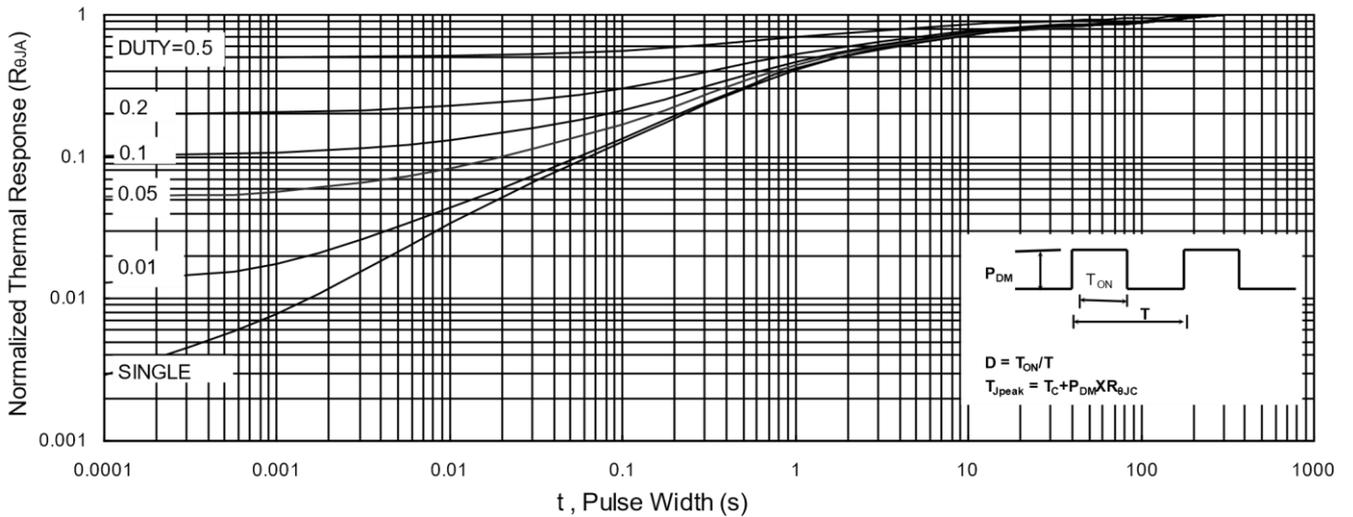
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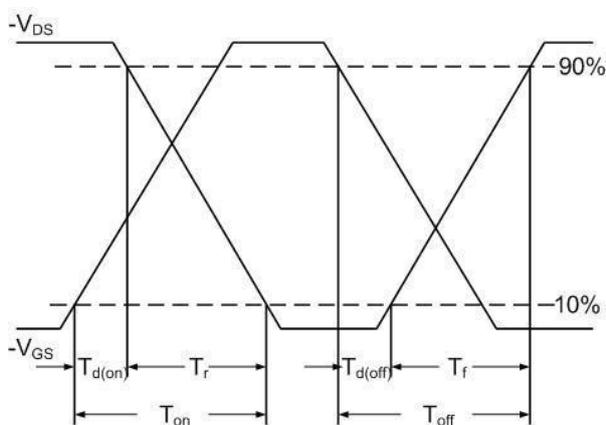
**Fig.7 Capacitance**



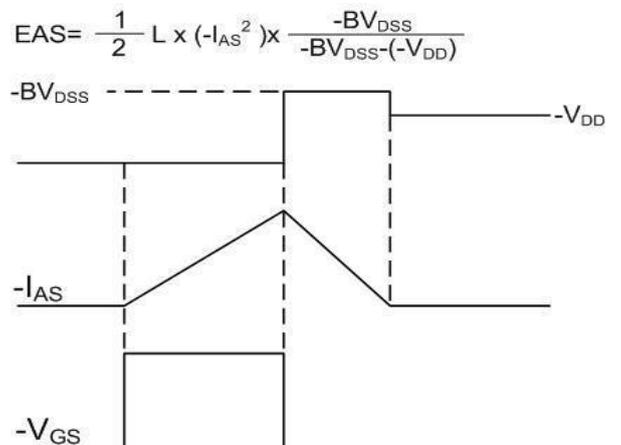
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

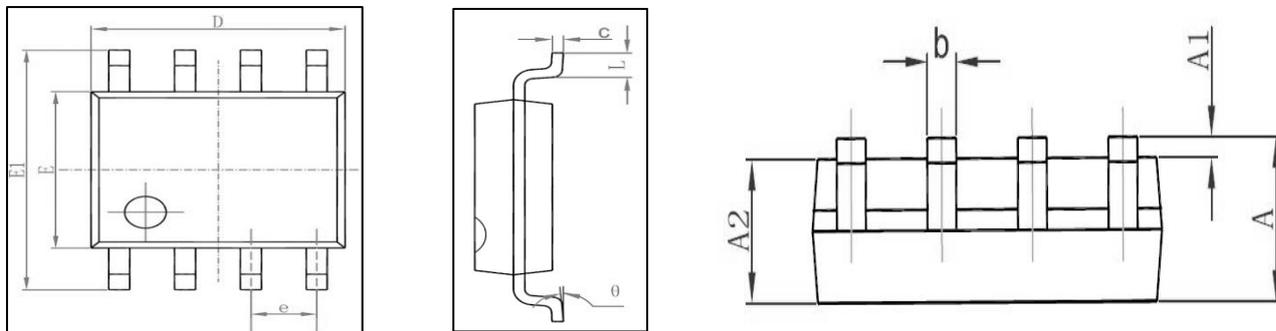


**Fig.10 Switching Time Waveform**

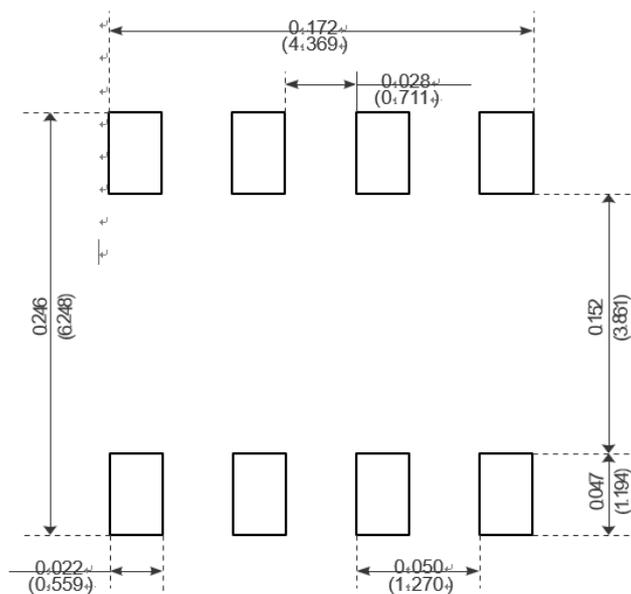


**Fig.11 Unclamped Inductive Switching Waveform**

### Package Mechanical Data-SOP-8/ESOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°



Recommended Minimum Pads

**30V N+P-Channel Enhancement Mode MOSFET****Attention**

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