

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP10G02S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 12A$

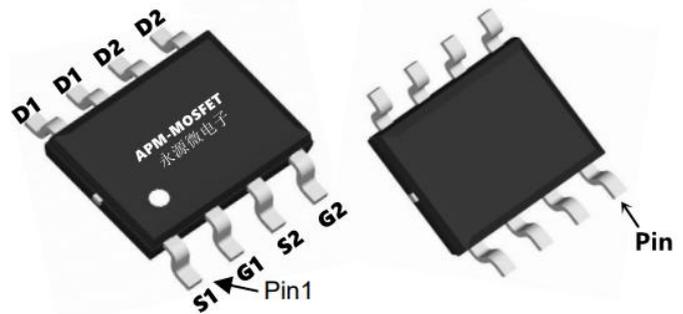
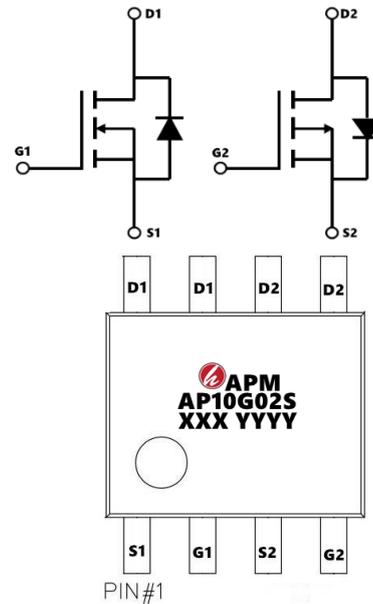
$R_{DS(ON)} < 20m\Omega$ @ $V_{GS}=10V$ (Type: **15m Ω**)

$V_{DS} = -20V$ $I_D = -9.8A$

$R_{DS(ON)} < 35m\Omega$ @ $V_{GS}=-10V$ (Type: **28m Ω**)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10G02S	SOP-8L	AP10G02S XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	12	-9.8	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.2	-5.5	A
I_{DM}	Pulsed Drain Current ²	36	-32	A
EAS	Single Pulse Avalanche Energy ³	85	78	mJ
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	3.5	3.5	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85		$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	50		$^\circ\text{C/W}$



20V N+P-Channel Enhancement Mode MOSFET

N-Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	22		V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.018	---	V/ $^{\circ}\text{C}$
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.50	0.65	1.0	V
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=4A$		15	20	m Ω
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS}=2.5V, I_D=3A$		20	35	
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
Ciss	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHz}$		888		pF
Coss	Output Capacitance			133		
Crss	Reverse Transfer Capacitance			117		
Qg	Total Gate Charge	$V_{GS}=4.5V, V_{DS}=10V, I_D=6.8A$		11.05		nC
Qgs	Gate-Source Charge			1.73		
Qgd	Gate-Drain Charge			3.1		
tD(on)	Turn-on Delay Time	$V_{GS}=4.5V, V_{DS}=10V,$ $I_D=6.8A$ $R_{GEN}=3\Omega$		7		ns
tr	Turn-on Rise Time			46		
tD(off)	Turn-off Delay Time			30		
tf	Turn-off fall Time			52		
VSD	Diode Forward Voltage	$I_S=4A, V_{GS}=0V$			1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

20V N+P-Channel Enhancement Mode MOSFET

P-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-20	-24	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-0.4	-0.7	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	V _{GS} = -4.5V, I _D = -4A	-	28	35	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	V _{GS} = -2.5V, I _D = -3A	-	35	42	mΩ
Ciss	Input Capacitance	V _{DS} = -10V, V _{GS} =0V, f=1.0MHz	-	830	-	pF
Coss	Output Capacitance		-	132	-	pF
Crss	Reverse Transfer Capacitance		-	85	-	pF
Q _g	Total Gate Charge	V _{DS} = -10V, I _D = -2A, V _{GS} = -4.5V	-	8.8	-	nC
Q _{gs}	Gate-Source Charge		-	1.4	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	1.9	-	nC
td(on)	Turn-on Delay Time	V _{DD} = -10V, I _D = -3.3A, R _G = 1Ω, V _{GEN} = -4.5V	-	10	-	ns
tr	Turn-on Rise Time		-	32	-	ns
td(off)	Turn-off Delay Time		-	50	-	ns
t _f	Turn-off Fall Time		-	51	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.1	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -4A	-	-	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

20V N+P-Channel Enhancement Mode MOSFET

N-Channel Typical Characteristics

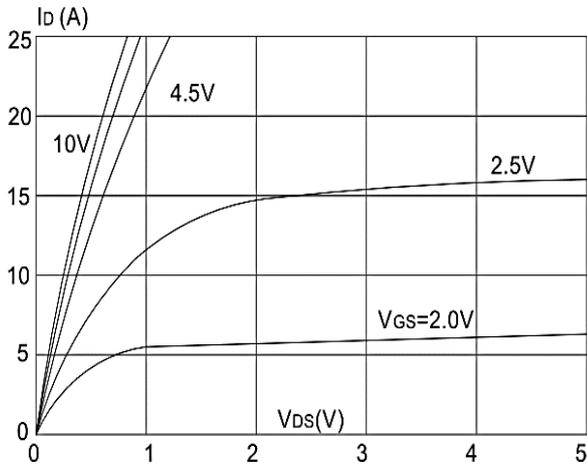


Figure 1: Output Characteristics

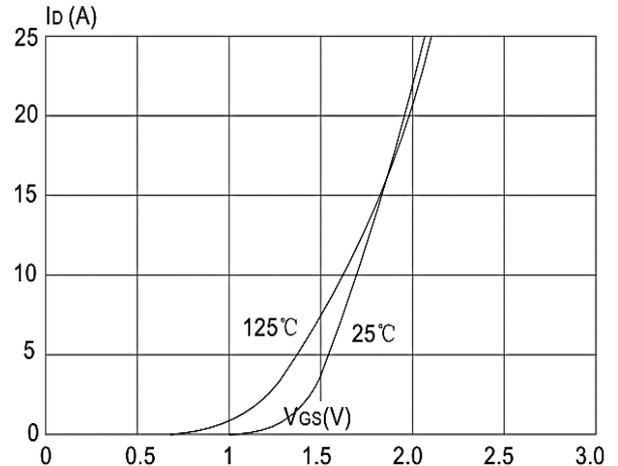


Figure 2: Typical Transfer Characteristics

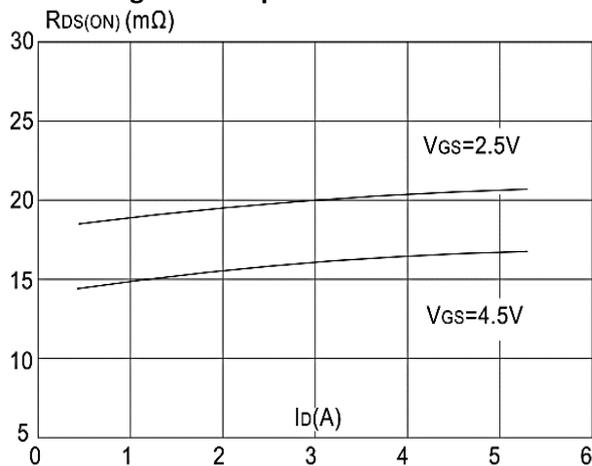


Figure 3: On-resistance vs. Drain Current

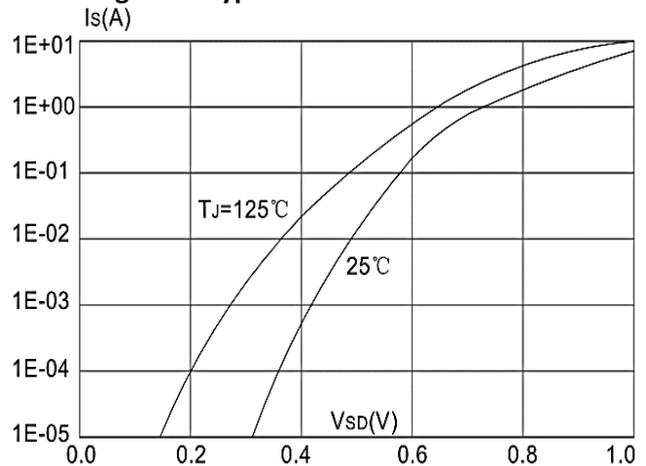


Figure 4: Body Diode Characteristics

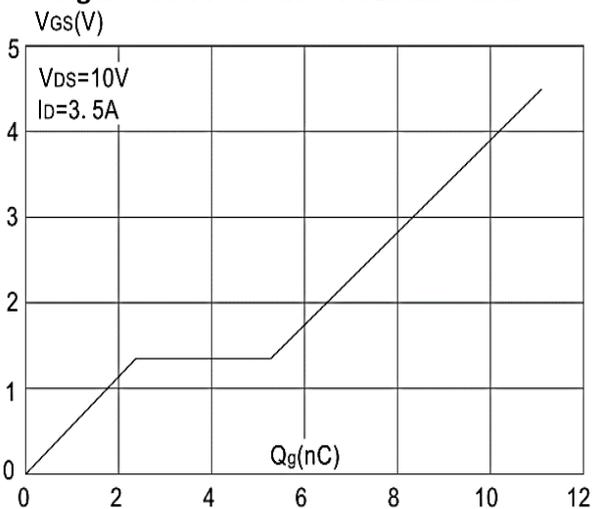


Figure 5: Gate Charge Characteristics

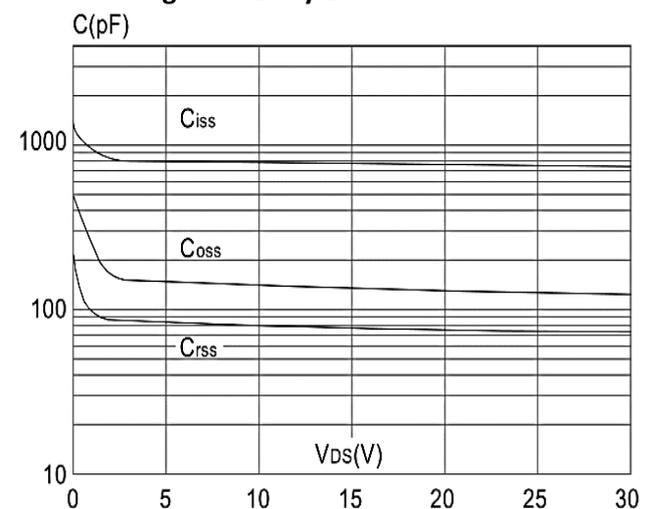


Figure 6: Capacitance Characteristics

20V N+P-Channel Enhancement Mode MOSFET

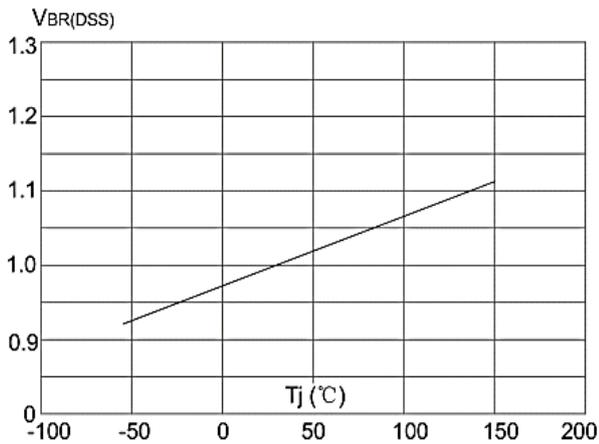


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

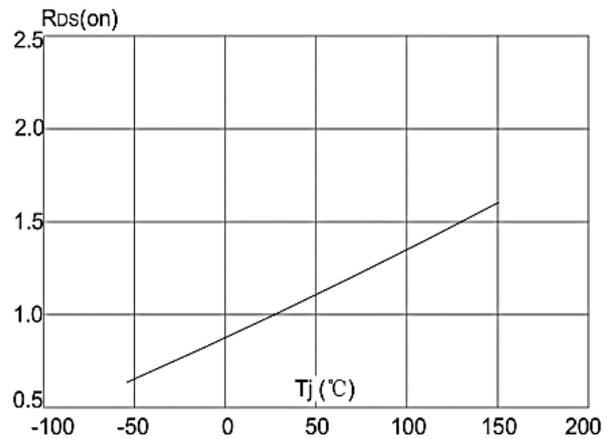


Figure 8: Normalized on Resistance vs. Junction Temperature

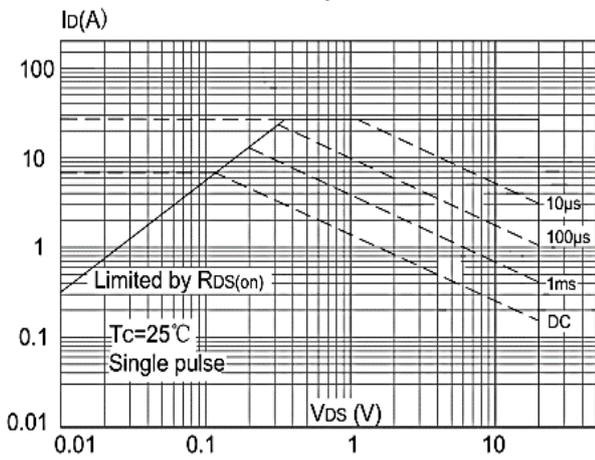


Figure 9: Maximum Safe Operating Area vs. Case Temperature

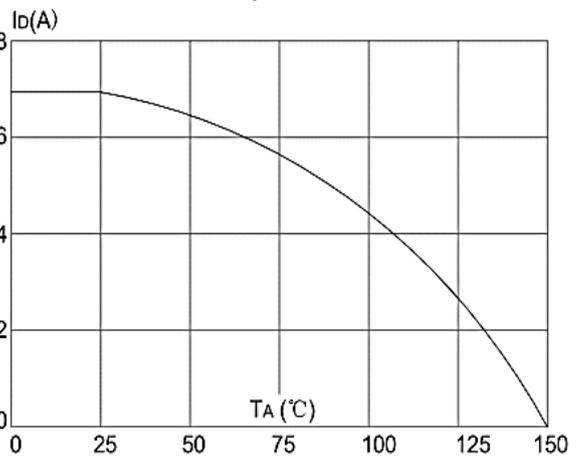


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

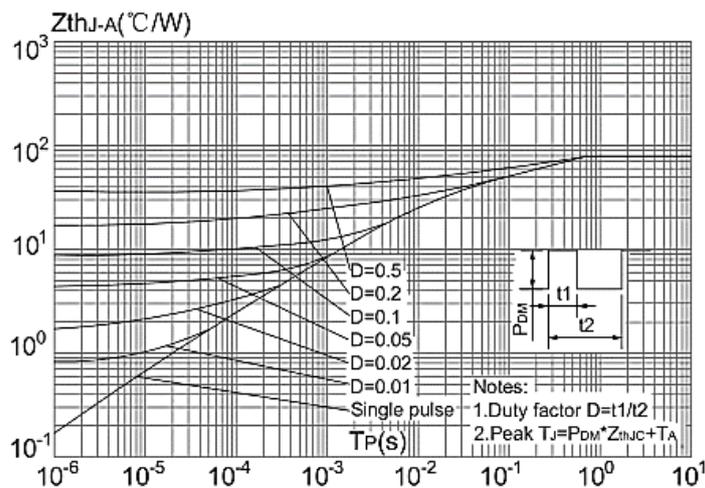


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

20V N+P-Channel Enhancement Mode MOSFET

P-Channel Typical Characteristics

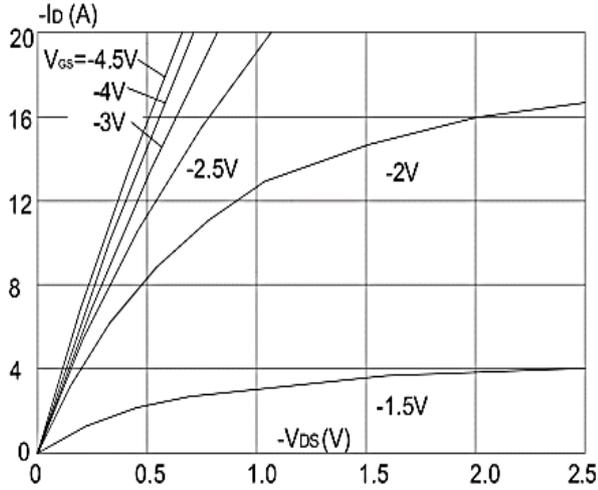


Figure 1: Output Characteristics

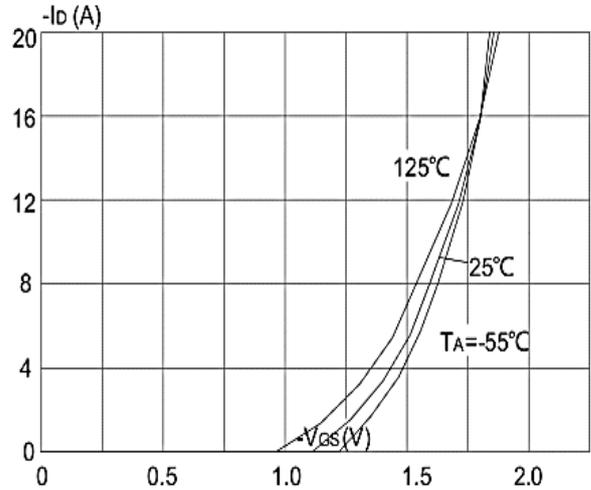


Figure 2: Typical Transfer Characteristics

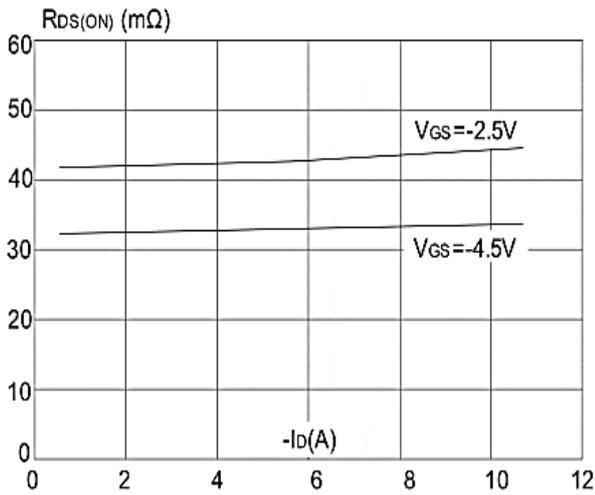


Figure 3: On-resistance vs. Drain Current

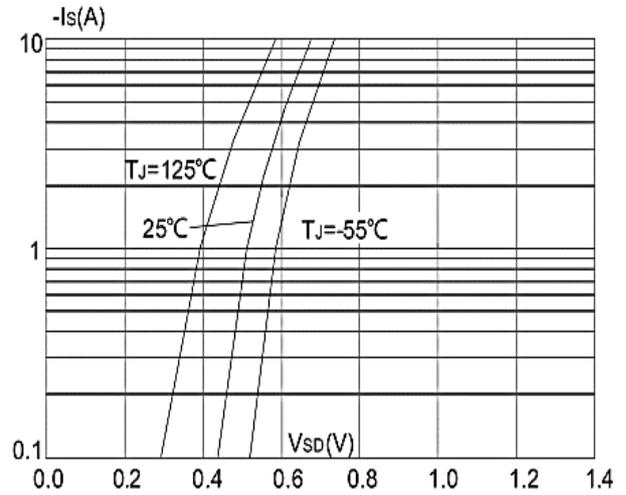


Figure 4: Body Diode Characteristics

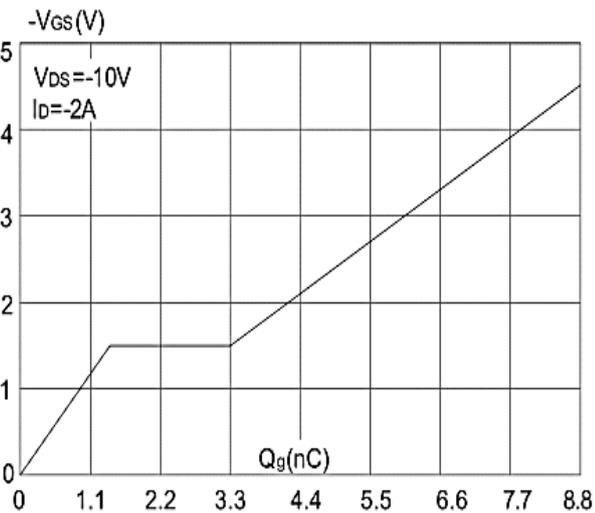


Figure 5: Gate Charge Characteristics

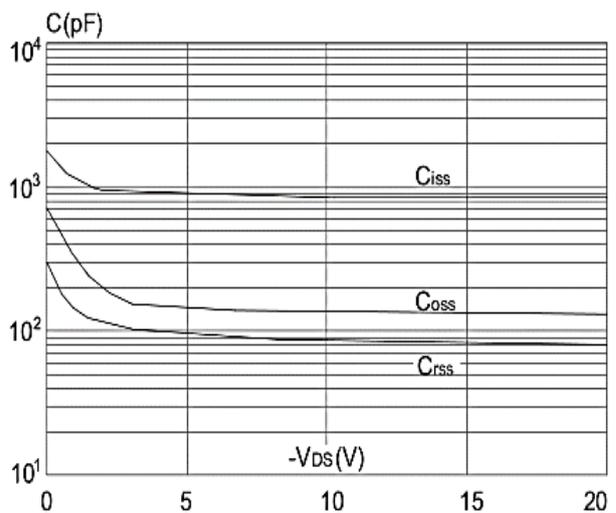


Figure 6: Capacitance Characteristics



20V N+P-Channel Enhancement Mode MOSFET

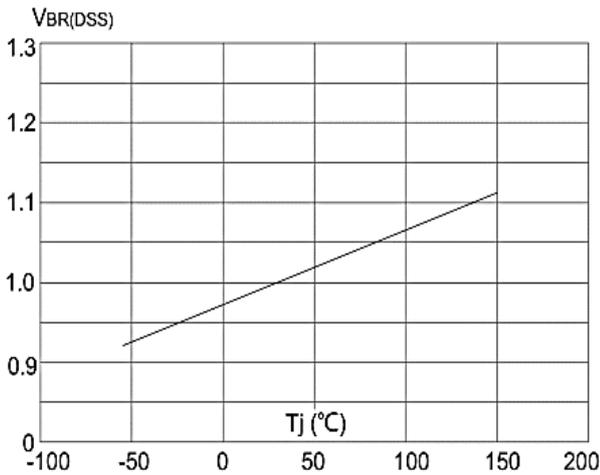


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

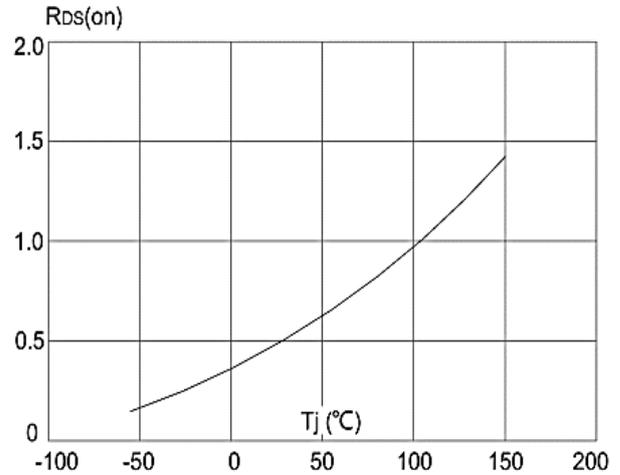


Figure 8: Normalized on Resistance vs. Junction Temperature

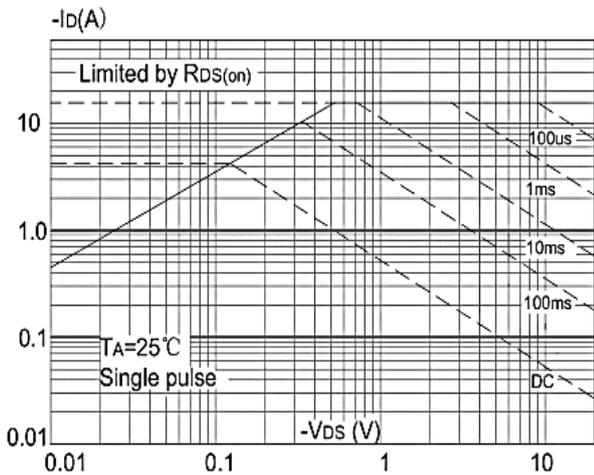


Figure 9: Maximum Safe Operating Area

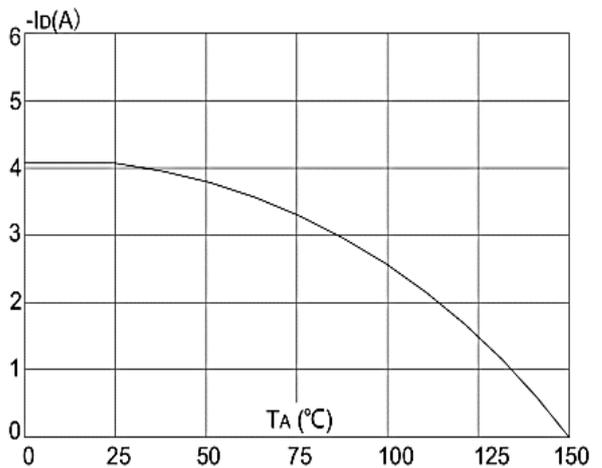


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

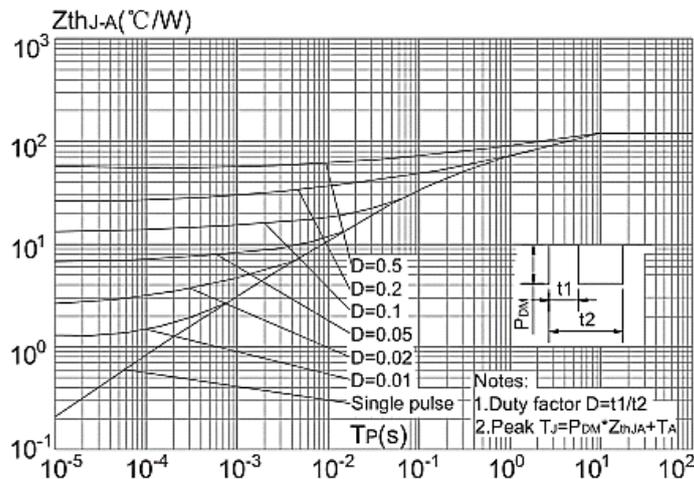
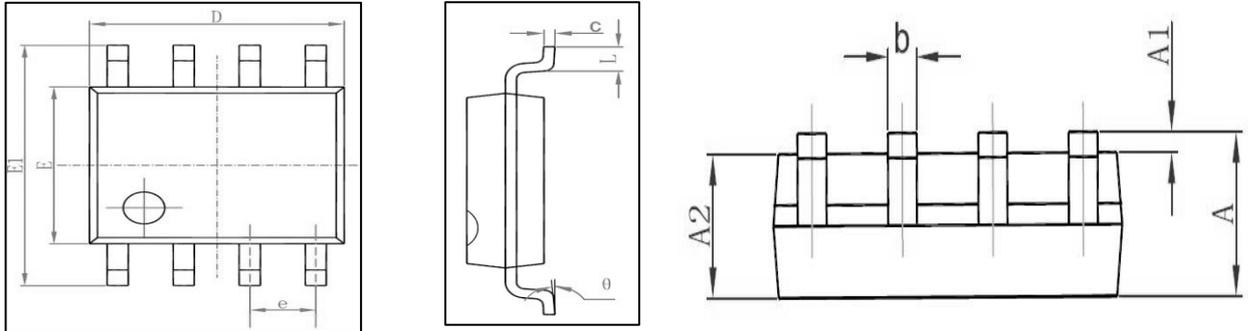


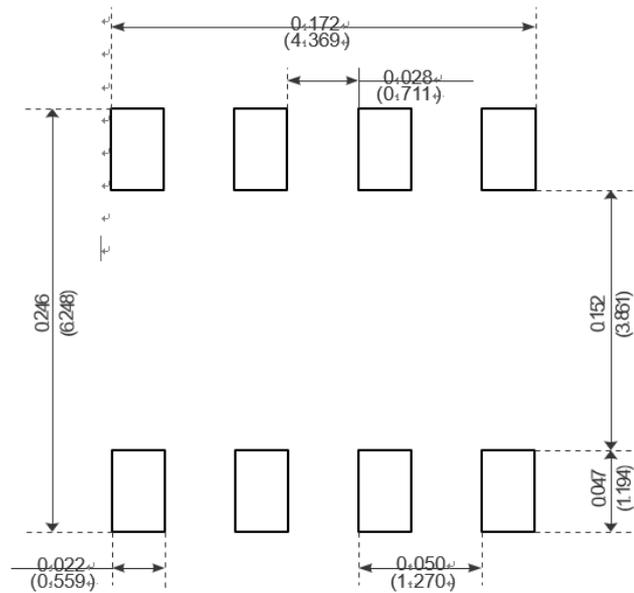
Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Package Mechanical Data-SOP-8L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

20V N+P-Channel Enhancement Mode MOSFET**Attention**

1, Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.

2, APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.

3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.

5, In the event that any or all APM Microelectronics products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.

6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.

7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you intend to use.

20V N+P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2021/12/21	Initial release

Copyright Attribution“APM-Microelectronice”