

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP10G02LI uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 12A$

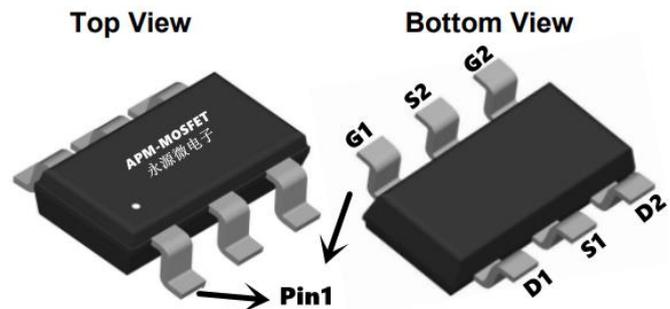
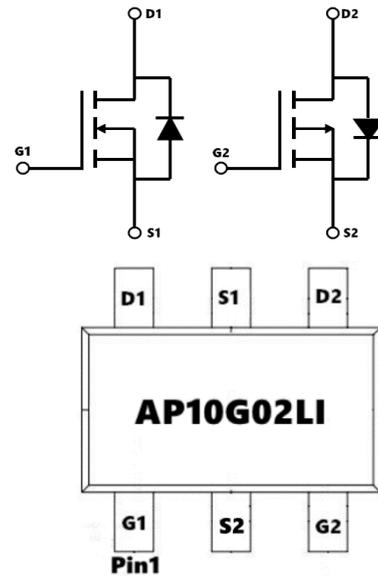
$R_{DS(ON)} < 20m\Omega$ @ $V_{GS}=10V$ (Type: **15mΩ**)

$V_{DS} = -20V$ $I_D = -9.8A$

$R_{DS(ON)} < 35m\Omega$ @ $V_{GS}=-10V$ (Type: **28mΩ**)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP10G02LI	SOT23-6L	AP10G02LI	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	12	-9.8	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.2	-5.5	A
I_{DM}	Pulsed Drain Current ²	36	-32	A
EAS	Single Pulse Avalanche Energy ³	85	78	mJ
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	3.5	3.5	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	105		$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	50		$^\circ\text{C}/\text{W}$



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N-Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BVDSS	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	22		V
$\Delta BVDSS/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.018	---	V/ $^{\circ}\text{C}$
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.50	0.65	1.0	V
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=7.6A$		15	20	m Ω
RDS(ON)	Static Drain-Source On-Resistance	$V_{GS}=2.5V, I_D=3.5A$		20	35	
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
Ciss	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHz}$		888		pF
Coss	Output Capacitance			133		
Crss	Reverse Transfer Capacitance			117		
Qg	Total Gate Charge	$V_{GS}=4.5V, V_{DS}=10V, I_D=6.8A$		11.05		nC
Qgs	Gate-Source Charge			1.73		
Qgd	Gate-Drain Charge			3.1		
tD(on)	Turn-on Delay Time	$V_{GS}=4.5V, V_{DS}=10V,$ $I_D=6.8A$ $R_{GEN}=3\Omega$		7		ns
tr	Turn-on Rise Time			46		
tD(off)	Turn-off Delay Time			30		
tf	Turn-off fall Time			52		
VSD	Diode Forward Voltage	$I_S=7.6A, V_{GS}=0V$			1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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P-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-20	-24	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-0.4	-0.7	-1.0	V
RDS(on)	Static Drain-Source on-Resistance note2	V _{GS} = -4.5V, I _D = -4.1A	-	28	35	mΩ
RDS(on)	Static Drain-Source on-Resistance note2	V _{GS} = -2.5V, I _D = -3A	-	35	42	mΩ
Ciss	Input Capacitance	V _{DS} = -10V, V _{GS} =0V, f=1.0MHz	-	830	-	pF
Coss	Output Capacitance		-	132	-	pF
Crss	Reverse Transfer Capacitance		-	85	-	pF
Q _g	Total Gate Charge	V _{DS} = -10V, I _D = -2A, V _{GS} = -4.5V	-	8.8	-	nC
Q _{gs}	Gate-Source Charge		-	1.4	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	1.9	-	nC
td(on)	Turn-on Delay Time	V _{DD} = -10V, I _D = -3.3A, R _G = 1Ω, V _{GEN} = -4.5V	-	10	-	ns
tr	Turn-on Rise Time		-	32	-	ns
td(off)	Turn-off Delay Time		-	50	-	ns
t _f	Turn-off Fall Time		-	51	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.1	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -4.1A	-	-	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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N-Channel Typical Characteristics

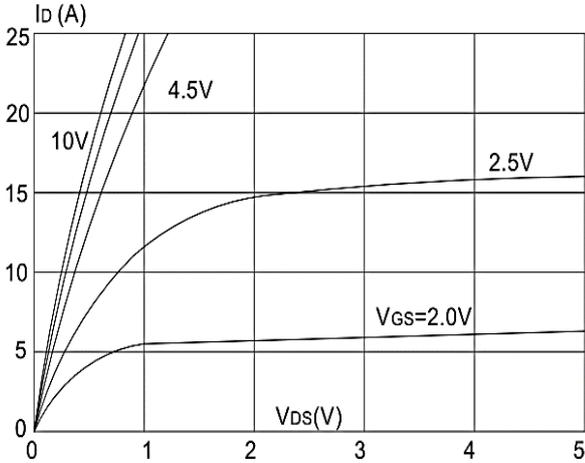


Figure 1: Output Characteristics

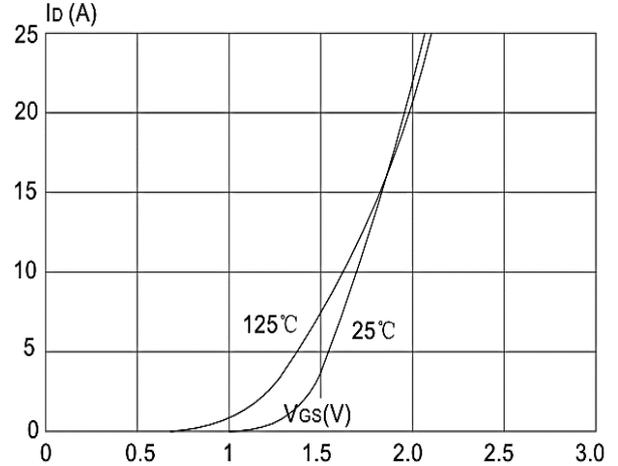


Figure 2: Typical Transfer Characteristics

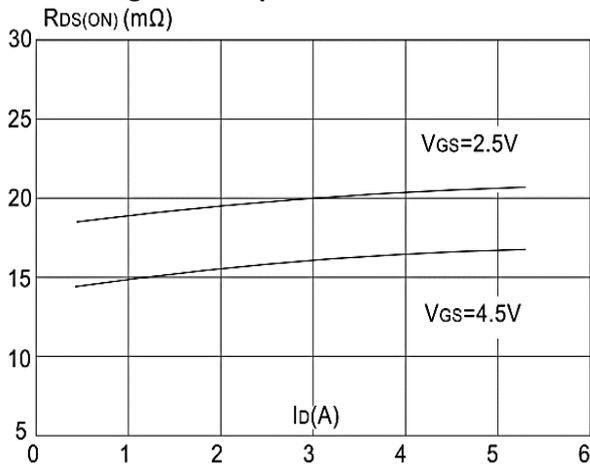


Figure 3: On-resistance vs. Drain Current

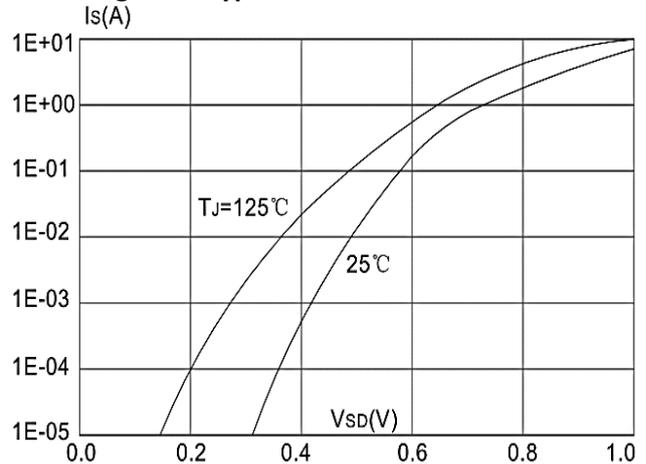


Figure 4: Body Diode Characteristics

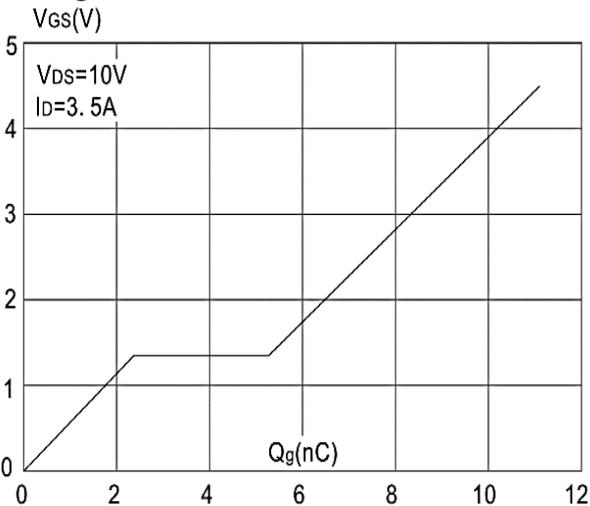


Figure 5: Gate Charge Characteristics

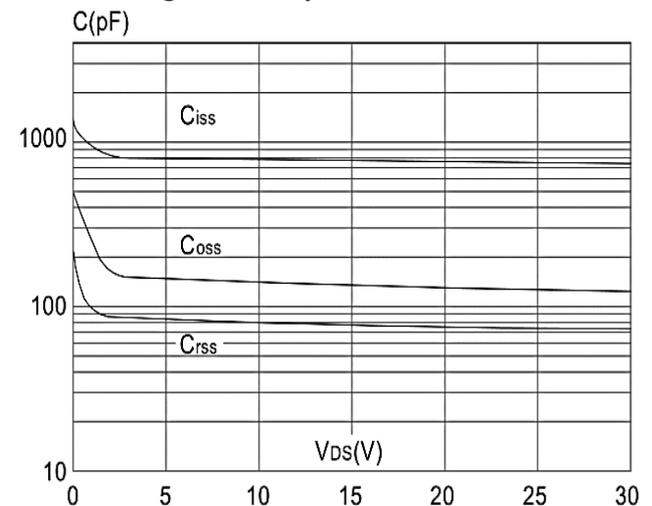


Figure 6: Capacitance Characteristics

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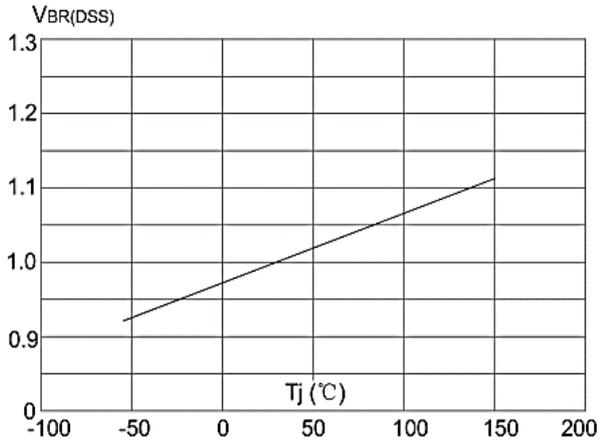


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

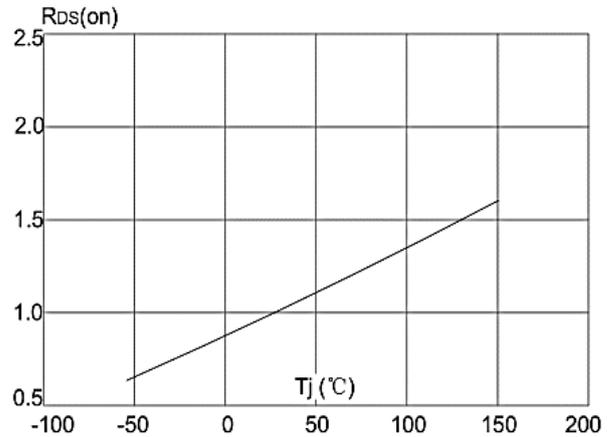


Figure 8: Normalized on Resistance vs. Junction Temperature

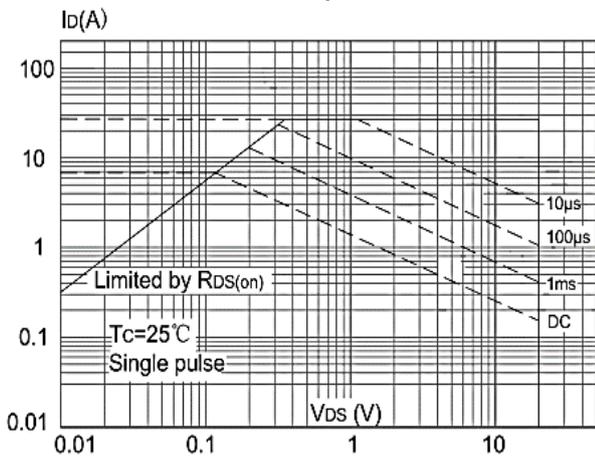


Figure 9: Maximum Safe Operating Area vs. Case Temperature

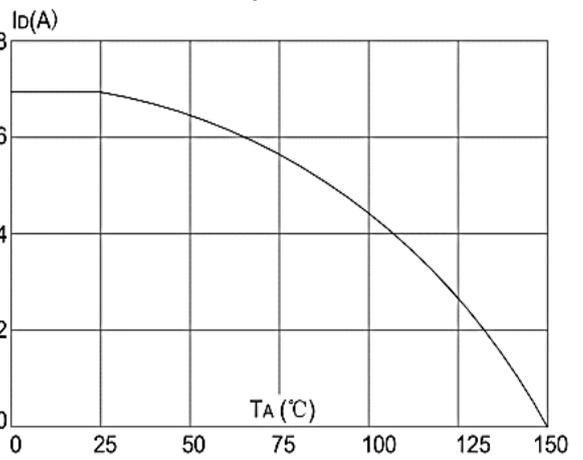


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

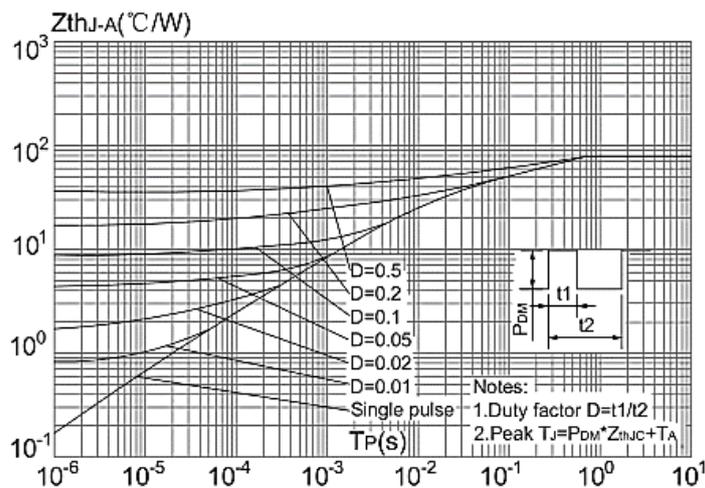


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

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P-Channel Typical Characteristics

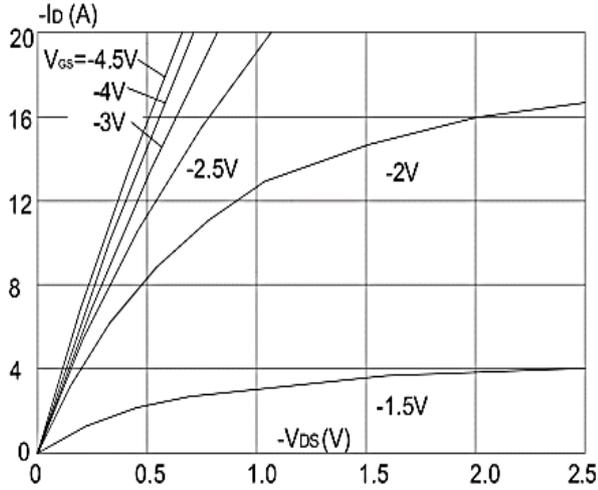


Figure 1: Output Characteristics

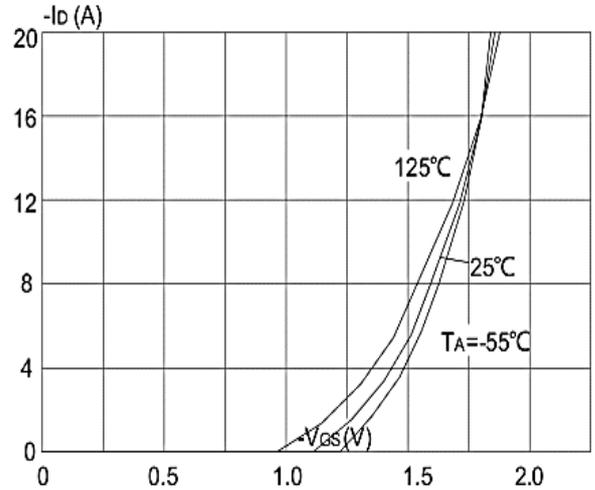


Figure 2: Typical Transfer Characteristics

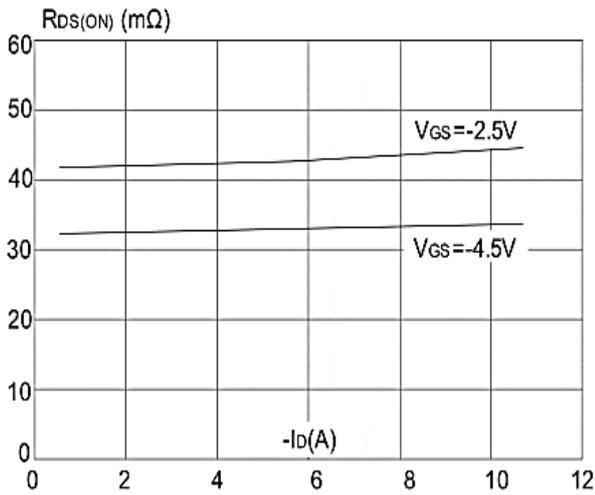


Figure 3: On-resistance vs. Drain Current

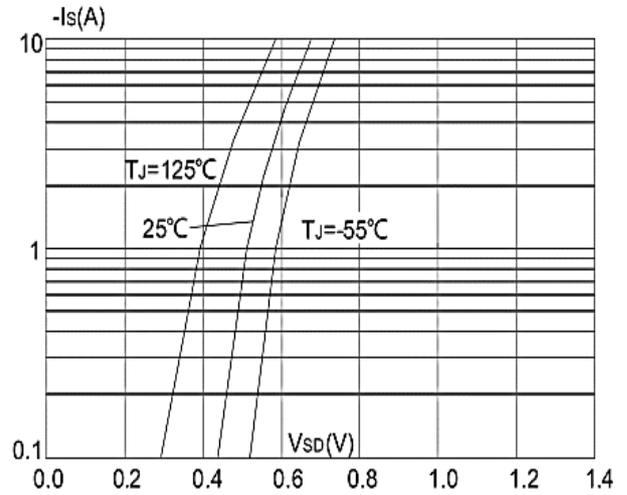


Figure 4: Body Diode Characteristics

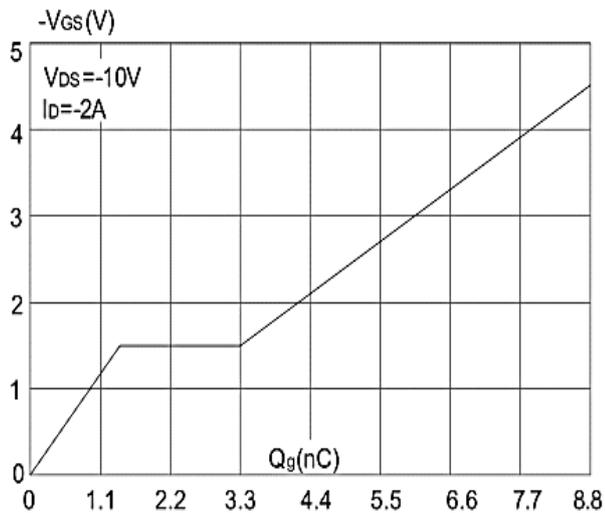


Figure 5: Gate Charge Characteristics

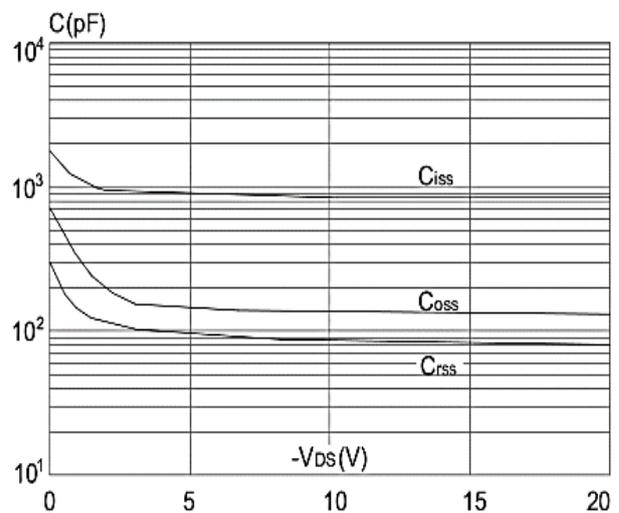


Figure 6: Capacitance Characteristics



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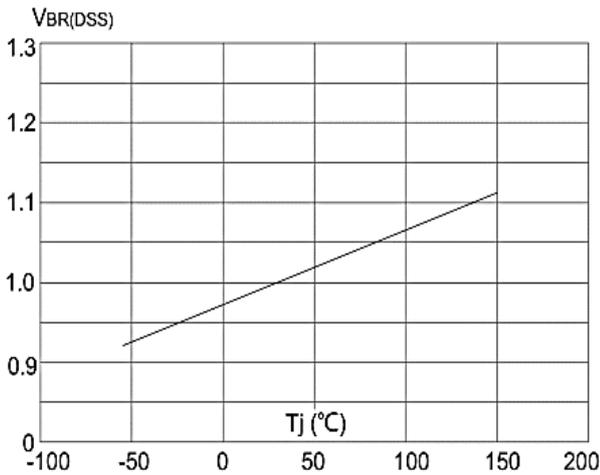


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

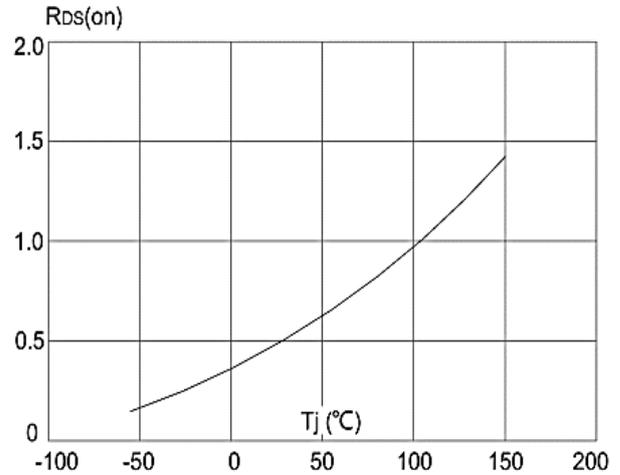


Figure 8: Normalized on Resistance vs. Junction Temperature

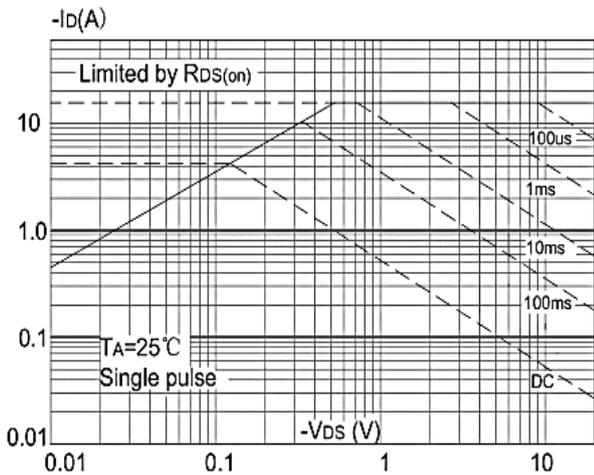


Figure 9: Maximum Safe Operating Area

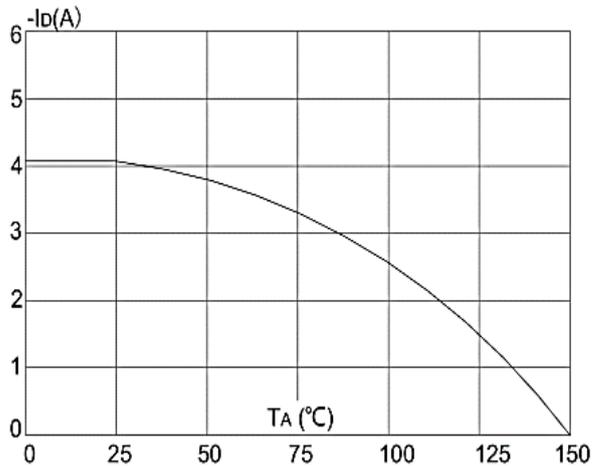


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

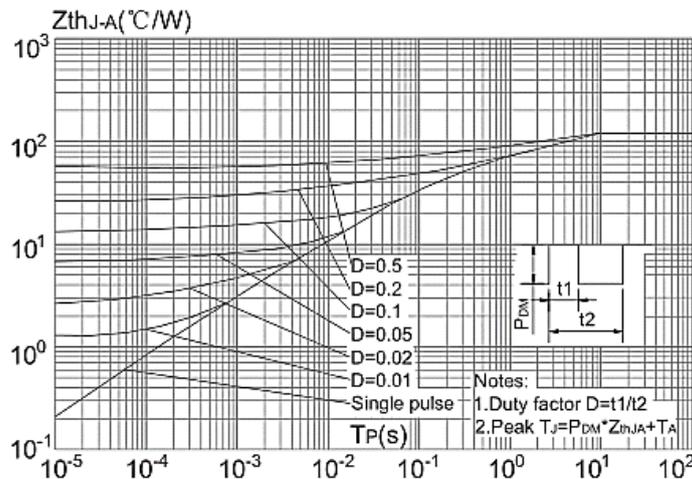
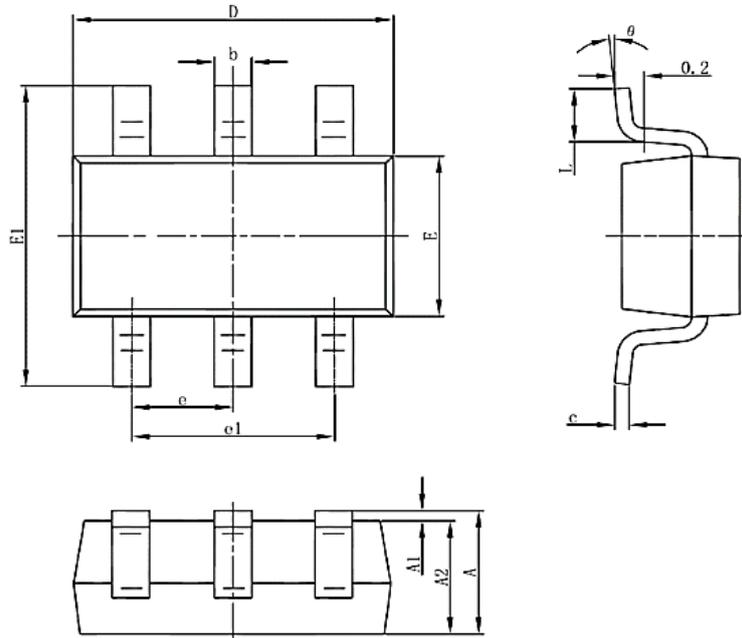


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Package Mechanical Data-SOT23-6-Double



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0	8	0	8

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2021/12/21	Initial release

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